

Raichu_WL / Pikachu_WL

Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

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<Core Design>

緯創資通

Wistron Corporation

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Title

Cover Page

Size
A4

Document Number

Raichu_WL/Pikachu_WL

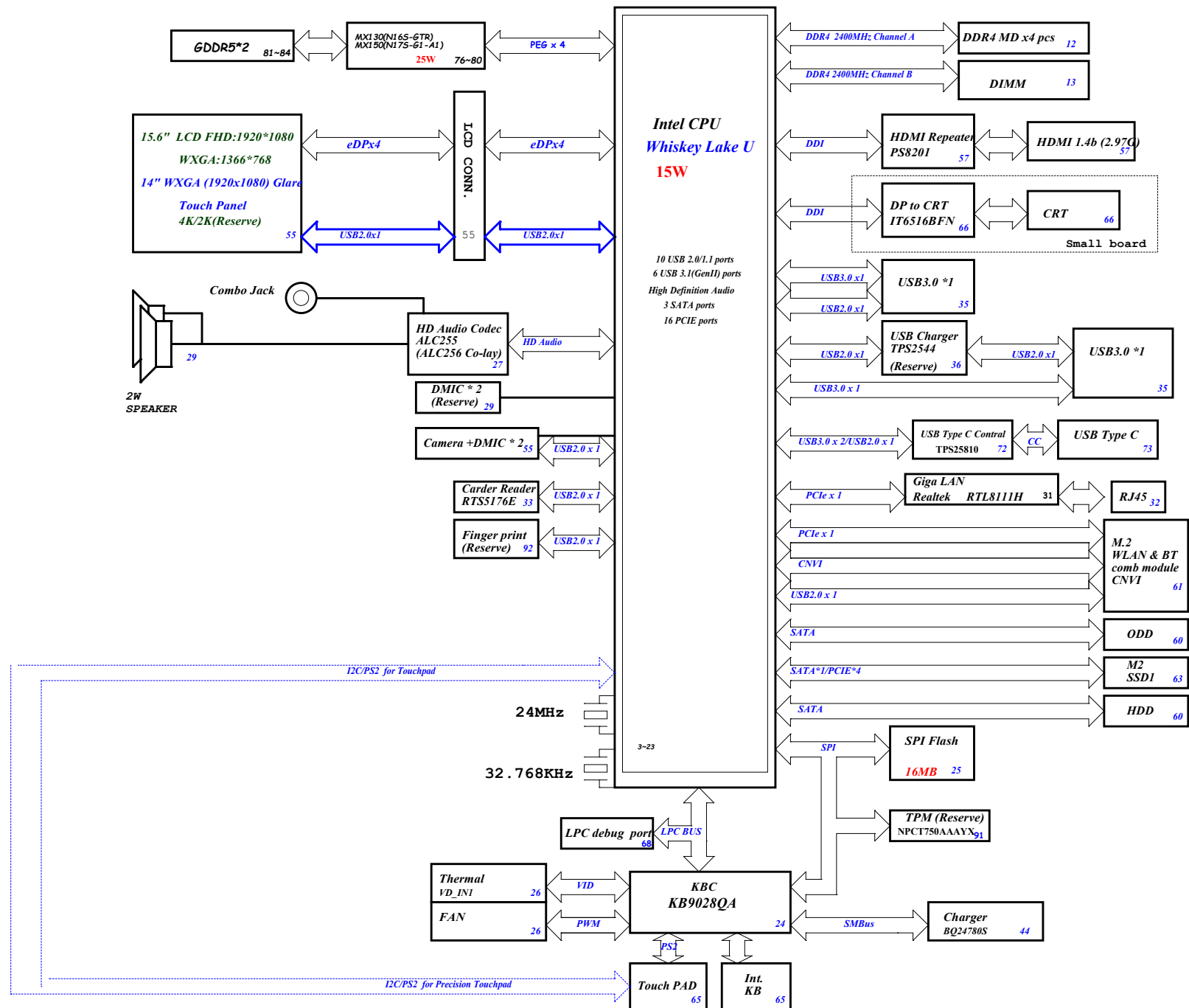
Rev
-1M

Date: Thursday, October 18, 2018

Sheet 1 of 106

Project Code:4PD0FT01A001 (14")
4PD0FZ010001 (15.6")
PCB No : 18730
Revision : -1M

Raichu_WL (14") / Pikachu_WL (15.6") Block Diagram



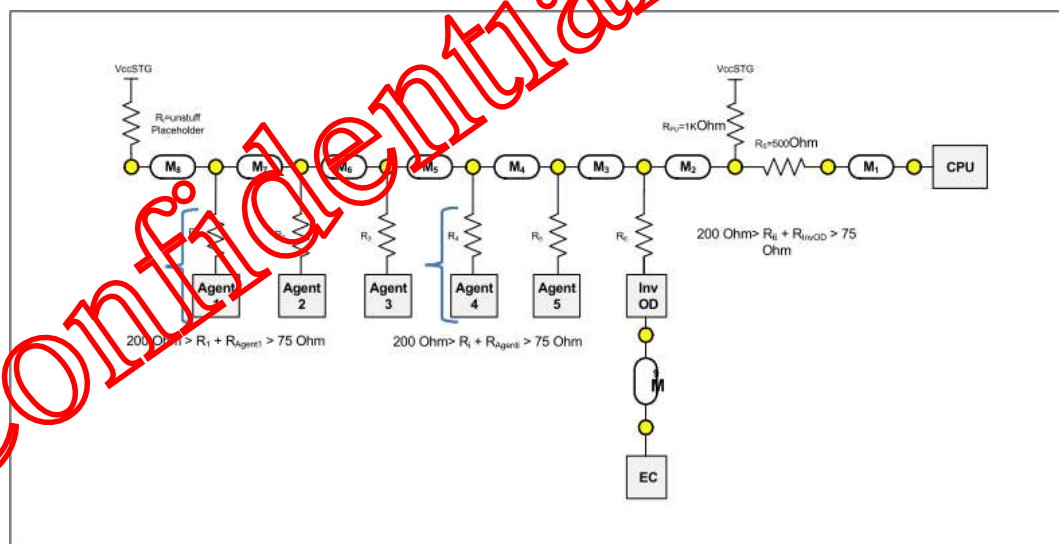
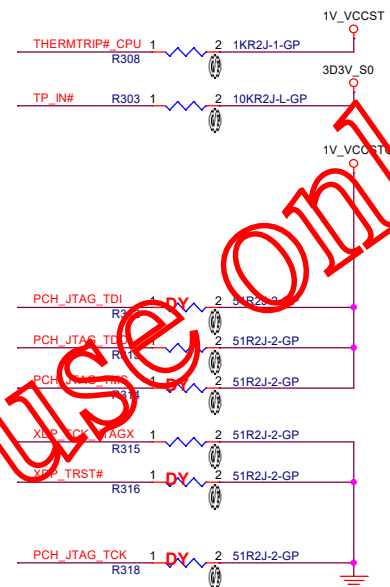
GPU DC/DC (N16S) RT8812A 85		CHARGER BQ24781 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1V_VGACORE_S0	3P_B*	19V_DCBATOUT
GPU DC/DC (N16S) AOZ2262QI-10-GP-U 86		SYSTEM DC/DC SY8180CRAC-GP 45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_VGA_S0	19V_DCBATOUT	5V_S5
GPU Load switch (N16S) G2898KD1U-GP 86		SYSTEM DC/DC SY8288BRAC-GP 45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0	19V_DCBATOUT	3D3V_S5
GPU Load switch (N16S) G2898KD1U-GP 86		CPU DC/DC RT3602 46-47	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_VGA_S0	19V_DCBATOUT	1V_CPU_CORE
GPU DC/DC (N16S) RT5797ALGQW-GP 86		CPU DC/DC SIC534CD-T1-GE3-GP 48	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1V_VGA_S0	19V_DCBATOUT	1V_VCCGT
GPU DC/DC (N17S) RT8816AGQW-GP 85		CPU DC/DC RT9610B 50	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1V_VGACORE_S0	19V_DCBATOUT	1V_VCCSA
GPU DC/DC (N17S) AOZ2262QI-10-GP-U 86		CPU DC/DC G5416QS1U-GP 51	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_VGA_S0	19V_DCBATOUT	PWR_VDDQ
GPU Load switch (N17S) G2898KD1U-GP 86		CPU DC/DC G5416QS1U-GP 51	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D8V_S5	1D8V_AON_S0	19V_DCBATOUT	2D5V_S3
GPU Load switch (N17S) G2898KD1U-GP 86		SYSTEM DC/DC AOZ2262QI-10-GP-U 52	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D8V_S5	1D8V_VGA_S0	19V_DCBATOUT	1D0V_S5
GPU DC/DC (N17S) RT5797ALGQW-GP 86		SYSTEM DC/DC APL5930KAI-TR6-1-GP 53	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1V_VGA_S0	3D3V_S5	1D8V_S5
		SYSTEM Load switch TPS22976 40	
		INPUTS	OUTPUTS
		3D3V_S5	3D3V_S0
		5V_S5	5V_S0
		1D0V_S5	1V_VCCST
		1D8V_S5	1D8V_S0
		SYSTEM Load switch APE8939 40	
		INPUTS	OUTPUTS
		1D0V_S5	1V_VCCIO

Vinafix

```

24  Peci_EC          << >>————
24,44,46 Pwr_Cpu_Prochot# << >>————
65  Tp_In#          >>————

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Title			
CPU (THML/JTAG)			
Size	Document Number		Rev
A3		Raichu_WL/Pikachu_WL	-1M
Date:	Tuesday, September 25, 2018	Sheet 3 of	106

SSID = CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU

24 eDP_BLEN_CPU
55 eDP_VDDEN_CPU
55 eDP_BLCtrl_CPU

HDMI

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 HDMI_SCL_CPU
57 HDMI_SDA_CPU

57 HDMI_DET_CPU

15 GPP_H17_STRAP

24 EC_SC#

DP to VGA

56 CRT_DDI_TX_N0
56 CRT_DDI_TX_P0
56 CRT_DDI_TX_N1
56 CRT_DDI_TX_P1

56 CRT_AUX_CPU_N
56 CRT_AUX_CPU_P

56 CRT_HPD_CPU

HDMI_DDI_TX_N2 AL5
HDMI_DDI_TX_P2 AL6
HDMI_DDI_TX_N1 AJ5
HDMI_DDI_TX_P1 AJ6
HDMI_DDI_TX_N0 AF6
HDMI_DDI_TX_P0 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6

CRT_DDI_TX_N0 AC4
CRT_DDI_TX_P0 AC3
CRT_DDI_TX_N1 AC1
CRT_DDI_TX_P1 AC2

AE4
AE3
AE1
AE2

CPU1A

DDI1_TXN0

DDI1_TXP0

DDI1_TXN1

DDI1_TXP1

DDI1_TXN2

DDI1_TXP2

DDI1_TXN3

DDI1_TXP3

DDI2_TXN0

DDI2_TXP0

DDI2_TXN1

DDI2_TXP1

DDI2_TXN2

DDI2_TXP2

DDI2_TXN3

DDI2_TXP3

GPP_E13/DDPB_HPD0/DISP_MISC0
GPP_E14/DDPC_HPD1/DISP_MISC1
GPP_E15/DDPB_HPD2/DISP_MISC2
GPP_E16/DDPB_HPD3/DISP_MISC3
GPP_E17/DDPB_HPD4/DISP_MISC4

EDP_BKLTEN
EDP_VDDEN
EDP_BKLTCTL

DISP_RCOMP

GPP_E18/DDPB_CTRLCLK/CNV_BT_HOST_WAKE#

GPP_E19/DDPB_CTRLCLK

GPP_E20/DDPB_CTRLCLK

GPP_E21/DDPB_CTRLCLK

GPP_E22/DDPB_CTRLCLK

GPP_E23/DDPB_CTRLCLK

GPP_H16/DDPB_CTRLCLK

GPP_H17/DDPB_CTRLCLK

WHISKEY-LAKE-GP

ZZ.00CPU.271

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4 eDP_TX_CPU_N2
AJ3 eDP_TX_CPU_P2
AJ2 eDP_TX_CPU_N3
AJ1 eDP_TX_CPU_P3

AH4 eDP_AUX_CPU_N
AH3 eDP_AUX_CPU_P

DISP_UTILS

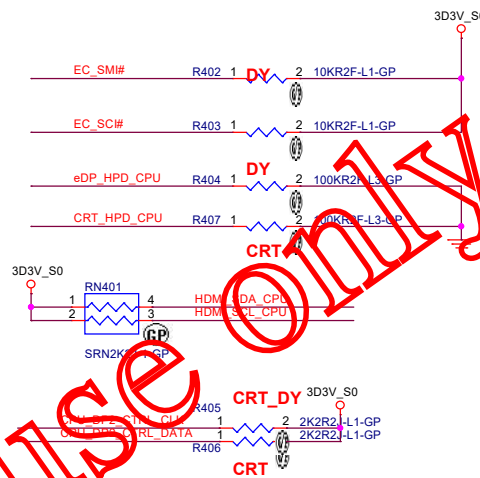
DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

CRT_AUX_CPU_N
CRT_AUX_CPU_P

AG7
AG6
AG5
AG4

CN6 HDMI_DET_CPU
CN6 CRT_HPD_CPU
CP7 EC_SM#
CP6 EC_SC#
CM7 eDP_HPD_CPU

CK11 eDP_BLEN_CPU
CS11 eDP_VDDEN_CPU
CH11 eDP_BLCtrl_CPU



eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistance Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω \pm 1%	600 mils

Note: Must maintain low DC resistance routing ($<0.1 \Omega$)

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Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DP	HDMIx_C_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_C_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_C_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_C_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_C_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_C_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_C_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_C_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CLK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA
	DDPB_CTRLCLK	NA	DDI1_CTRL_CLK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA
	DDPB_CTRLCLK	NA	DDI1_CTRL_CLK

Document Number: 575412 Ver 0.9 (Schematic Checklist)

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Title CPU (DDI/EDP)

Size A3 Document Number Raichu_WL/Pikachu_WL Rev -1M

Date: Tuesday, September 25, 2018 Sheet 4 of 106

SSID = CPU

DDR4 ball type: Interleaved Type

NIL

IL

DDR4

Document Number: 575414 Ver 1.2

12 M_A_DQS_DN0
12 M_A_DQS_DP0
12 M_A_DQS_DN1
12 M_A_DQS_DP1
12 M_A_DQS_DN2
12 M_A_DQS_DP2
12 M_A_DQS_DN3
12 M_A_DQS_DP3
12 M_A_DQS_DN4
12 M_A_DQS_DP4
12 M_A_DQS_DN5
12 M_A_DQS_DP5
12 M_A_DQS_DN6
12 M_A_DQS_DP6
12 M_A_DQS_DN7
12 M_A_DQS_DP7

12 M_A_DQ0
12 M_A_DQ1
12 M_A_DQ2
12 M_A_DQ3
12 M_A_DQ4
12 M_A_DQ5
12 M_A_DQ6
12 M_A_DQ7
12 M_A_DQ8
12 M_A_DQ9
12 M_A_DQ10
12 M_A_DQ11
12 M_A_DQ12
12 M_A_DQ13
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12 M_A_DQ63

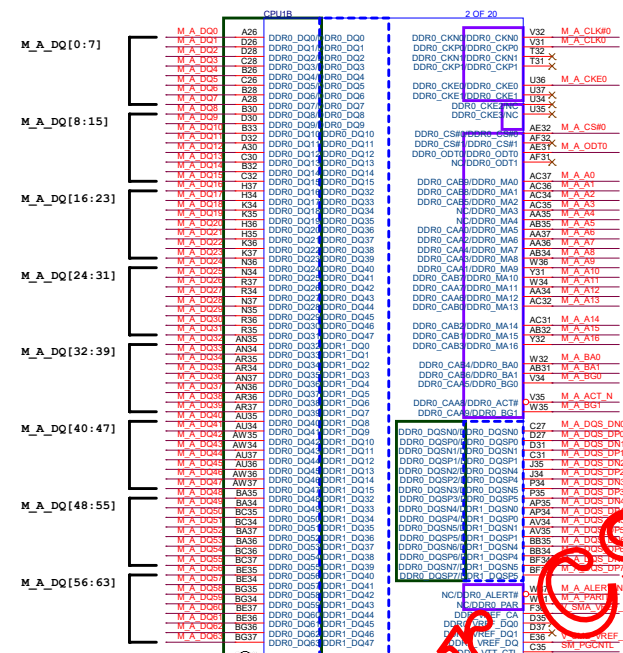
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12 M_A_CS0
12 M_A_ODT0
12 M_A_A0
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12 M_A_A2
12 M_A_A3
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12 M_A_A10
12 M_A_A11
12 M_A_A12
12 M_A_A13
12 M_A_A14
12 M_A_A15
12 M_A_ACT_N
12 M_A_BG0
12 M_A_BG1
12 M_A_BA0
12 M_A_BA1
12 M_A_ALERT_N
12 M_A_PARITY
12 V_SMA_VREF_CA
12 V_SMA_VREF_CB
12,13 SM_DRAMRST#

51 VTT_CNTL

13 M_B_DQS_DN0
13 M_B_DQS_DP0
13 M_B_DQS_DN1
13 M_B_DQS_DP1
13 M_B_DQS_DN2
13 M_B_DQS_DP2
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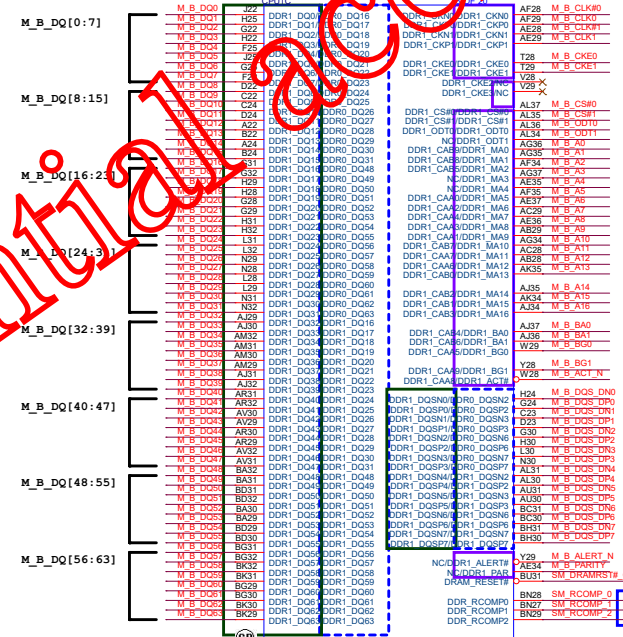
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13 M_B_ODT1
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13 M_B_A6
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13 M_B_A8
13 M_B_A9
13 M_B_A10
13 M_B_A11
13 M_B_A12
13 M_B_A13
13 M_B_A14
13 M_B_A15
13 M_B_ACT_N
13 M_B_BG0
13 M_B_BG1
13 M_B_BA0
13 M_B_BA1
13 M_B_ALERT_N
13 M_B_PARITY



WHISKEY-LAKE-GP

ZZ.00CPU.271



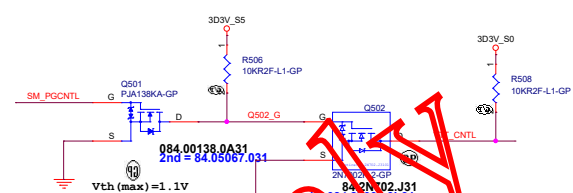
WHISKEY-LAKE-GP

ZZ.00CPU.271

Notes:

1. Avoid any parallel routing for Memory down x16 Channel and SoDIMM Channel.
2. For CFL-U43e/WHL-U42 Rcomp[0] should be 121 Ohm. For CNL-U22 all RCOMP value 100 Ohm

Document Number: 575412 Ver 0.9



084.00138.0A31

2nd = 84.08067.031

Vth(max)=1.1V

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CPU (DDR)

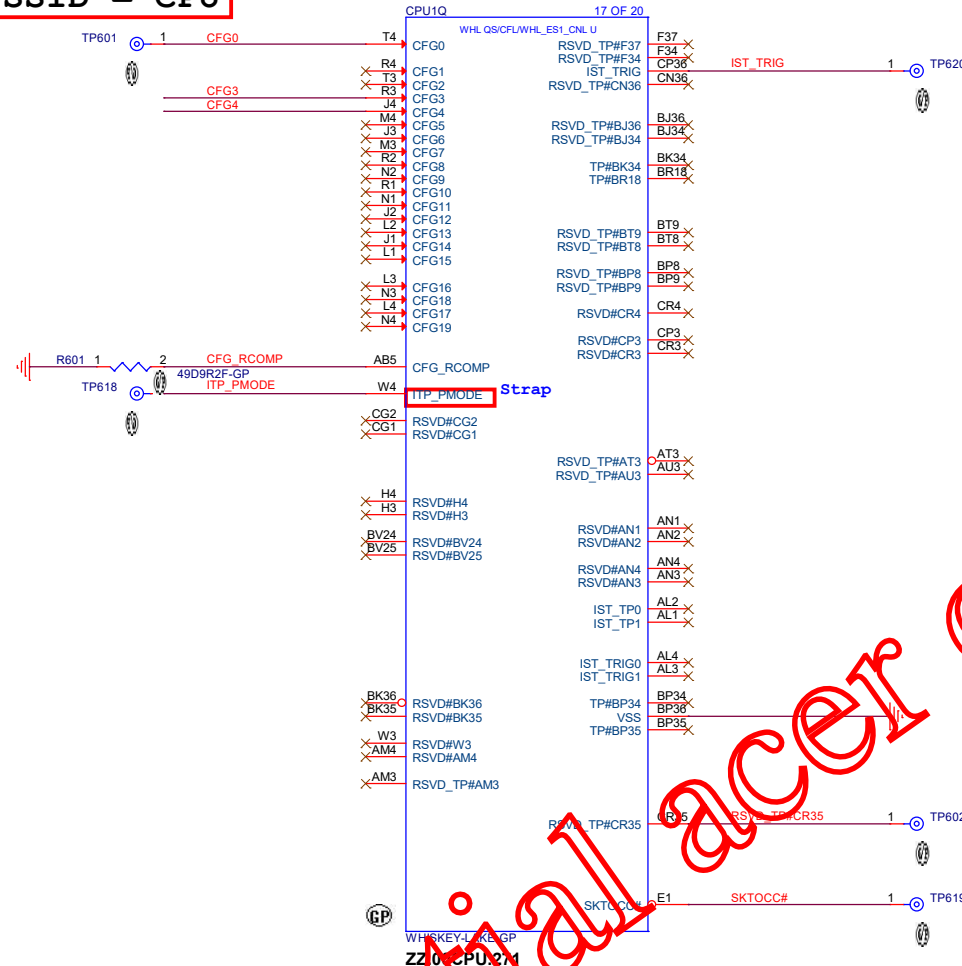
Raichu W/Pikachu_WL

Rev

Date: Tuesday, September 25, 2018

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SSID = CPU



Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none">• CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none">— 1 = (Default) Normal Operation; No stall.— 0 = Stall.• CFG[1]: Reserved configuration lane.• CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">— 1 = Normal operation— 0 = Lane numbers reversed• CFG[3]: Reserved configuration lane.• CFG[4]: eDP enable:<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">— 00 = 1x8, 2x4 PCI Express*— 01 = reserved— 10 = 2x8 PCI Express*— 11 = 1x16 PCI Express*• CFG[7]: PEG Training:<ul style="list-style-type: none">— 1 = (default) PEG Train immediately following RESET# de assertion.— 0 = PEG Wait for BIOS for training.• CFG[19:8]: Reserved configuration lanes.		GTL	SE	U - Processor Lines: CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.

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CFG Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		
CFG[1]	Reserved. No connect			
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation 0 = Lane numbers reserved		
CFG[3]	Reserved configuration lane			
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0: Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1	
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*		
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.	1	
CFG[19:8]	Reserved configuration lands.			

Document Number: 575412 Ver 0.9 (Schematic Checklist)

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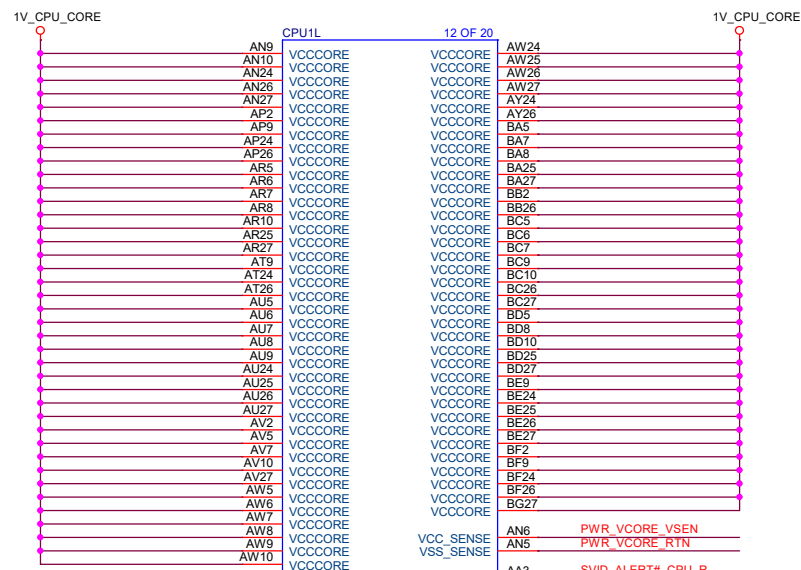
Title	CPU (CFG/IST)		
Size	Document Number	Raichu_WL/Pikachu_WL	Rev -1M
Date:	Tuesday, September 25, 2018	Sheet 6	of 106

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46 PWR_VCORE_VSEN      <<=====
46 PWR_VCORE_RTN       <<=====

46 PWR_VCORE_ALERT#    >>=====
46 VIDSCK_CPU_R        >>=====
46 VIDSOUT_CPU_R       <<>>=====

```



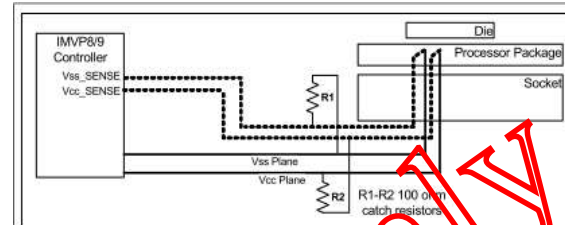
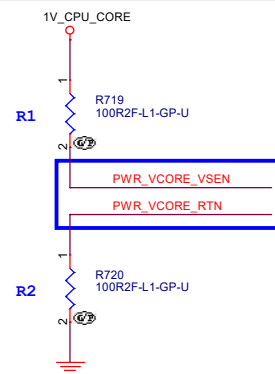
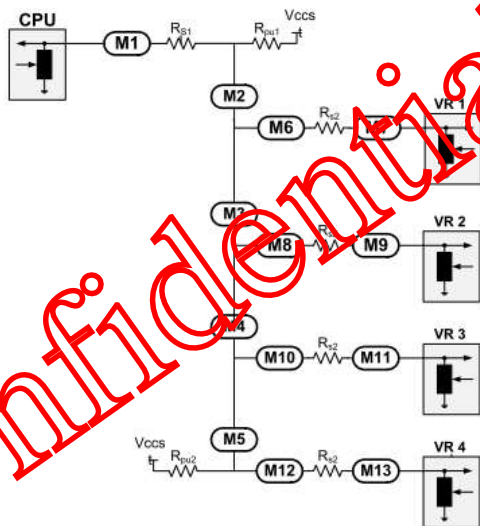
Document Number: 575418 Ver 1.0
Vcc 70A(Max)

BB9 RSVD#BB9
~~BC24~~ RSVD#BC24
~~AY9~~ RSVD#AY9
~~BB24~~ RSVD#BB24

GP

WHISKEY-LAKE-GP

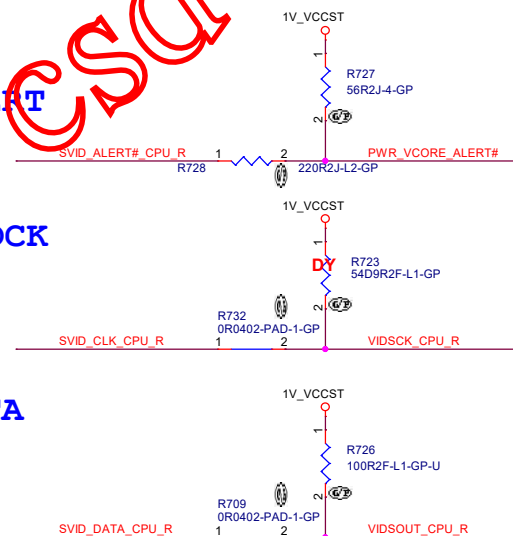
ZZ.00CPU.271



Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccSA_SENSE / VssSA_SENSE		NA	
VccIO_SENSE / VssIO_SENSE ⁽¹⁾			

R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc SENSE/Vss SENSE line resistance.

Document Number: 575412 Ver. 0.



SVID ALERT

~~SWID CLOCK~~

SVID DATA

SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

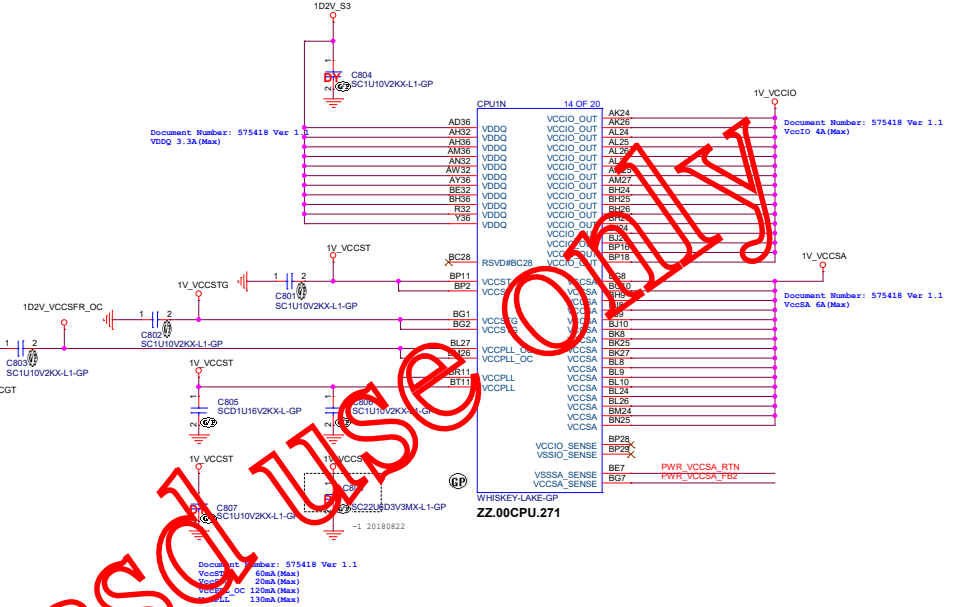
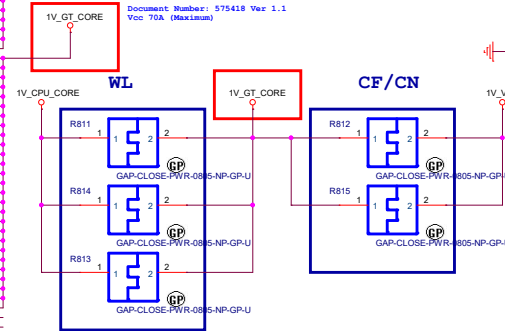
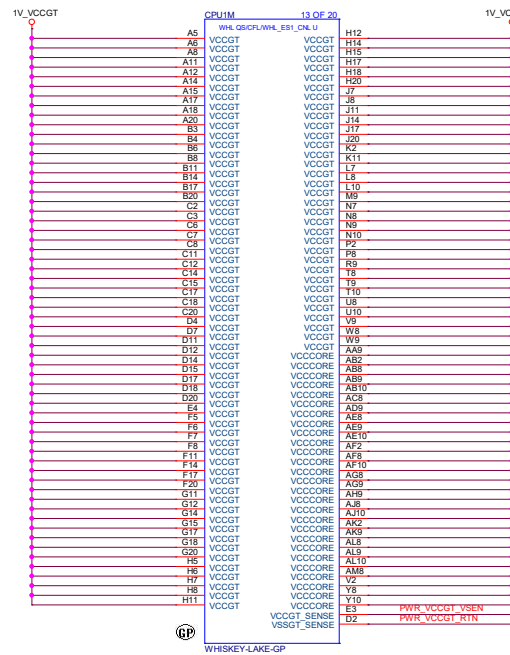
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Title				CPU (VCORE/MD)			
Size	Document Number					Rev	
A3	Raichu_WL/Pikachu_WL					-1M	
Date:	Tuesday, September 25, 2018			Sheet	7	of	106

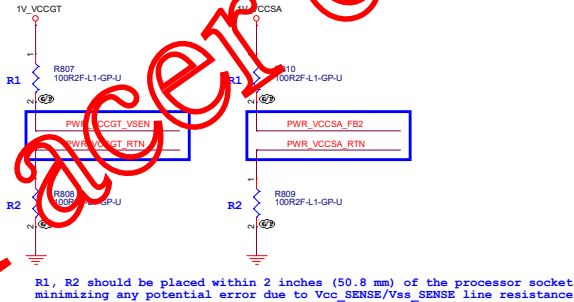
46 PWR_VCCGT_VSEN
46 PWR_VCCGT_RTIN
46 PWR_VCCSA_FB2
46 PWR_VCCSA_RTIN



Date	Revision	Ball#	Description	Old Name	New Name
01/Nov/2017	1.0		Initial revision	Initial revision	Initial revision
22/Dec/2017	1.1	AA9, AB10, AB2, AB8, AB9, AC3, AD9, AE10, AE8, AE9, AF10, AF2, AF8, AG8, AG9, AH9, AJ10, AJ8, AK2, AK9, AL10, AL8, AL9, AM8, V2, Y10, Y8	VCCGT	VCCORE	VCCGT
	1.2	AL1, AL2, AL3, AL4, AM3, AT3, AU3, BJ34, BJ36, BF8, BF9, BT8, BT9, CR35, CF25	IST_TP[1], IST_TP[0], IST_TRIG[1], IST_TRIG[0], RSVD_TP, GPP_H21	RSVD, RSVD, RSVD, RSVD, RSVD, GPP_H21	IST_TP[1], IST_TP[0], IST_TRIG[1], IST_TRIG[0], RSVD_TP, GPP_H21

Bulk Decoupling Locations		Example		Notes
VCCORE	Power Plane at VR output	4x 220uF (@4.5mΩ ESR)		Placed at primary side near to VR output
VCCGT	Power Plane at VR output	2x 220uF (@4.5mΩ ESR)		Placed at primary side near to VR output
Domain	Primary Side cap	Secondary Side cap	Placement guideline	
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the BGA pins.	
		14x 10uF 0402		
		9x 22uF 0603		
	8x 10uF 0402		Place as close to the package as possible	
VCCGT	18x 47uF 0805 (6.3V)		Place as close to the package as possible	
	15x 22uF 0603		Place as close to the package as possible	
	4x 47uF 0805 (6.3V)		Place as close to the package as possible	
	15x 10uF 0402		Place as close to the package as possible	
VCCIO		4x 10uF 0402	Placeholder only.	
		2x 10uF 0402		
	6x 0.1uF 0402			
	2x 4.7uF 0805 (6.3V)			
VCCSA			Placeholder Only	
	2x 4.7uF 0805 (6.3V)			

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE	1x 22uF 0603	4x 1uF 0402/0201	Place as close to the package as possible.
VCCIO	6x 10uF 0402	3x 10uF 0402	Place as close to the package as possible.
VCCSA	4x 0.1uF 0402	1x 1uF 0402	Place as close to the package as possible.
VCCGT	1x 1uF 0402	1x 1uF 0402	Placeholder Only.
VCCST	1x 0.1uF 0201	1x 1uF 0402	Do not merge VCCST, VCCSTG and VCCGT to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCSTG	1x 1uF 0402	1x 1uF 0402	Place as close as possible to BGA.
VCCSF	1x 1uF 0402	1x 1uF 0402	Place as close as possible to BGA and can be placed on as either Primary or backside cap.
VCCIO	1x 1uF 0402	1x 0805	Placeholder Only. Can be placed on as either Primary or backside cap.
VCCSA	1x 1uF 0402		
VCCGT	1x 1uF 0402		



R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Document Number: 575418 Ver 1.2

Document Number: 575418 Ver 1.1

Document Number: 575418 Ver 1.1

Document Number: 575418 Ver 1.1

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Title

CPU (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

Rev
-1M

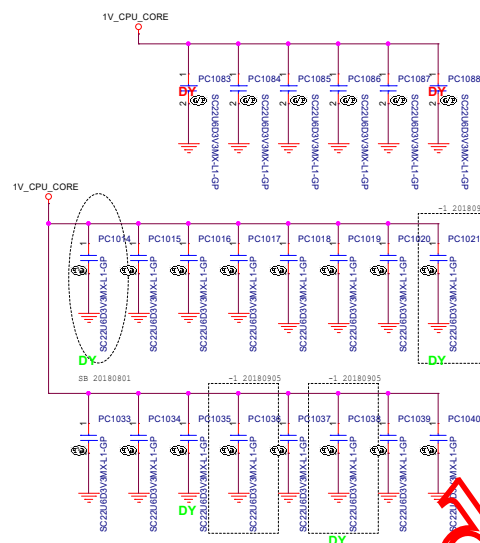
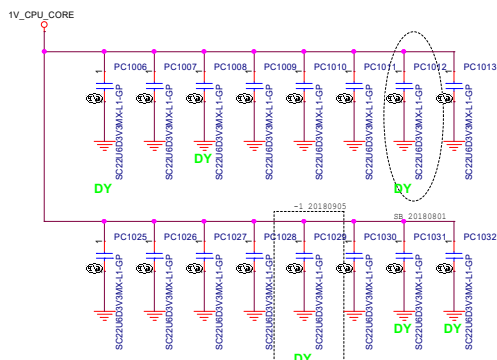
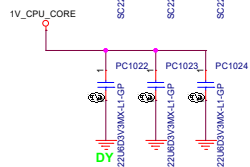
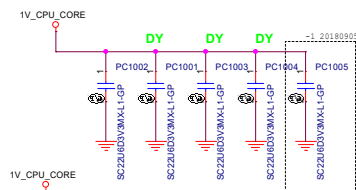
Date: Tuesday, September 25, 2018

Sheet 9 of 106

VCORE

U42
IccMax current-10ms max = 70 A

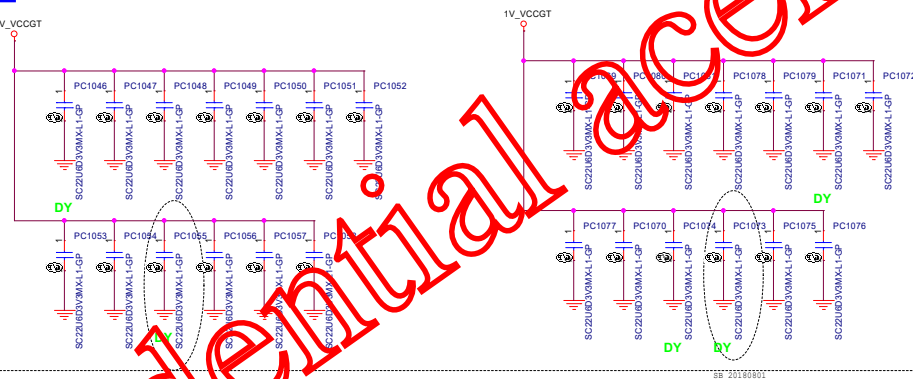
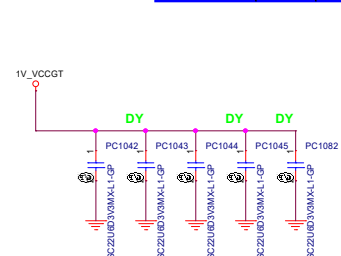
22uF	PCS	Cap
U42	33	330uF*2



WHL U42

U42
IccMax current-10ms max = 31 A

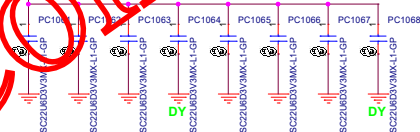
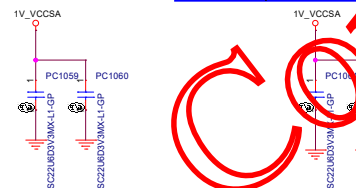
22uF	PCS	Cap
RT	25	330uF*1



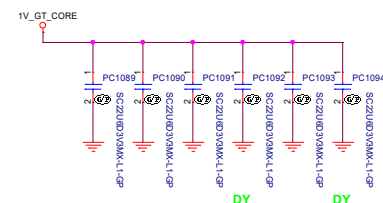
WHL U42

U42
IccMax current-10ms max = 5 A

22uF	PCS
RT	8



GT CORE



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Figure 1

CPU_(Power CAP1)

Size

Document Number

Cus

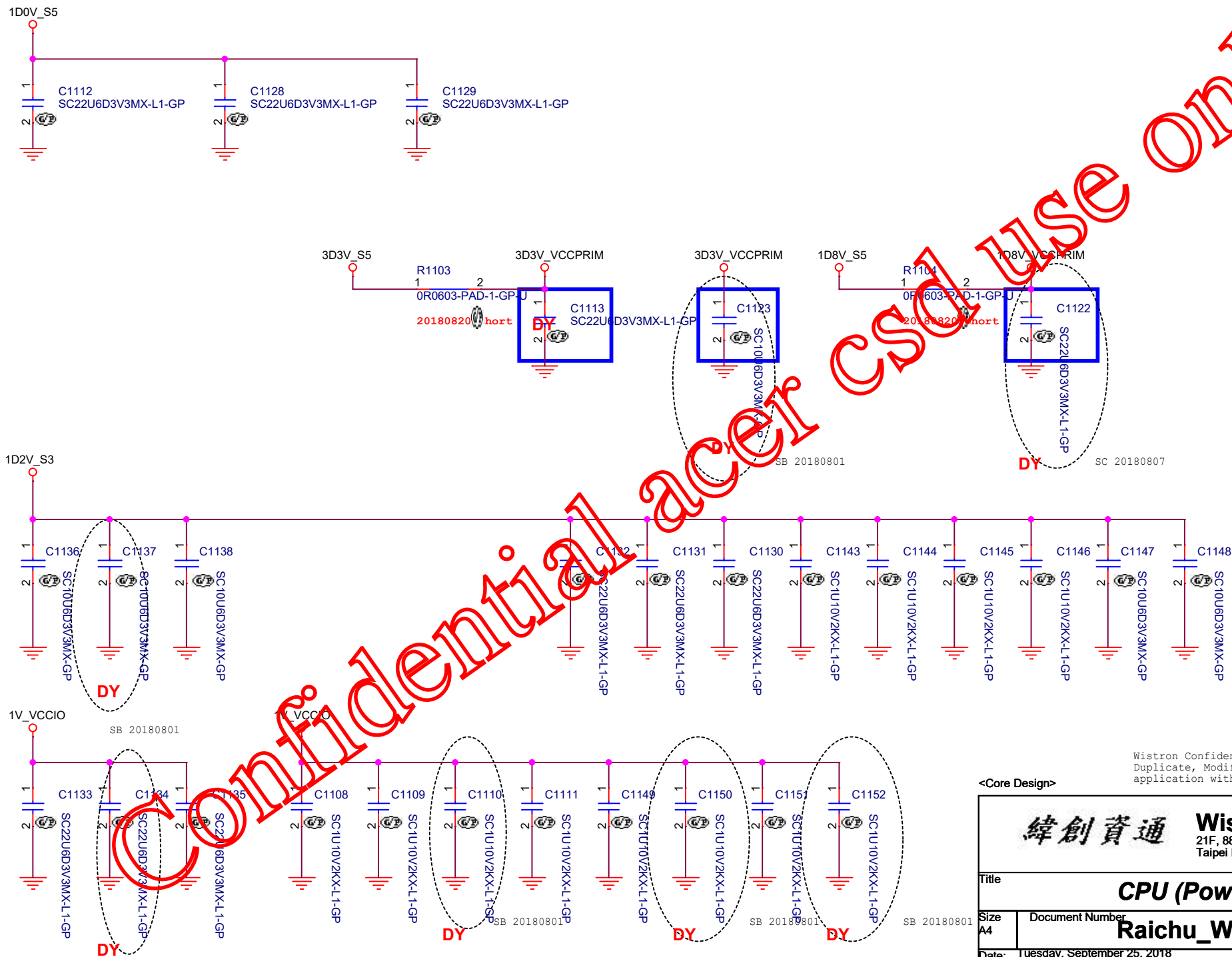
Raic

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SSID = PCH



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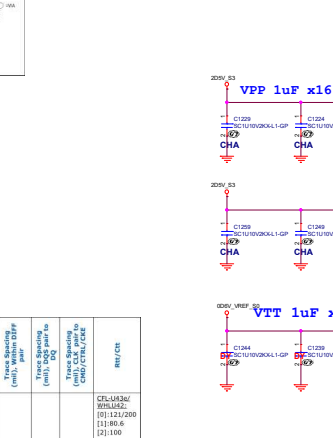
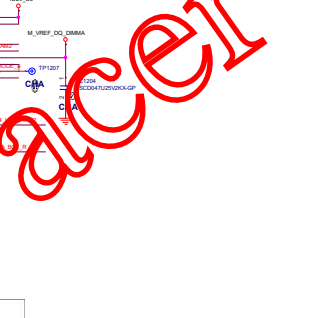
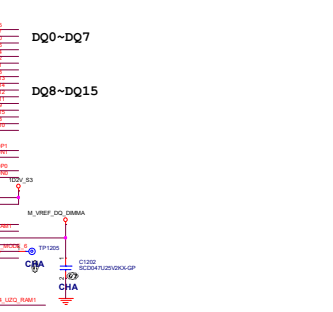
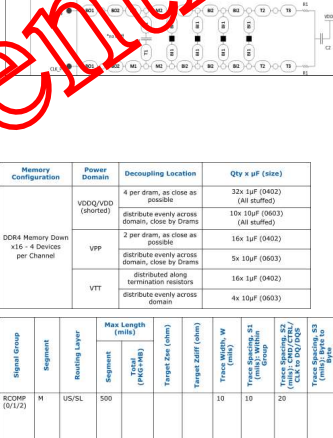
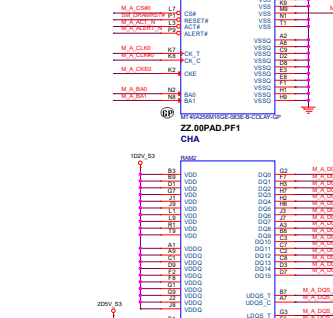
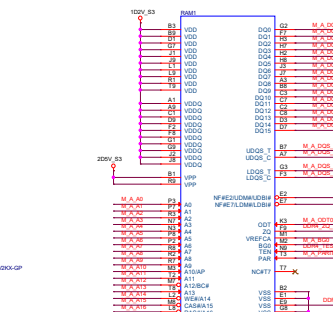
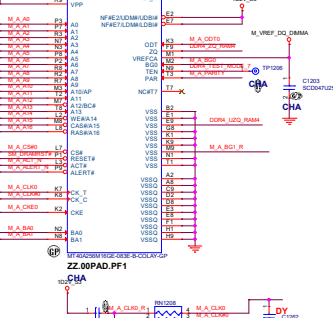
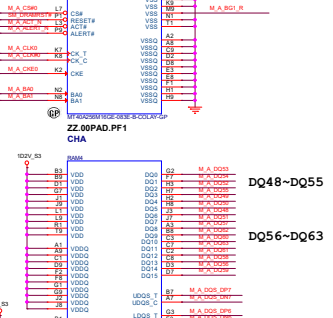
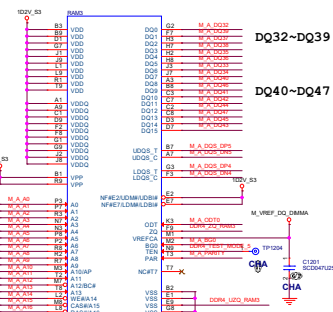
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Title			CPU (Power Cap2)	
Size A4	Document Number	Raichu_WL/Pikachu_WL		Rev -1M
Date:	Tuesday, September 25, 2018		Sheet 11	of 106

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

The diagram shows the pinout of the AD9288 ADC. The pins are numbered 1 through 31. The connections are as follows:

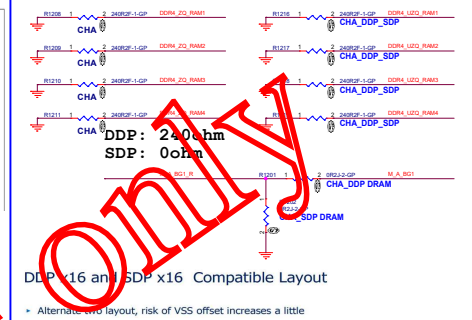
- VDDQ:** Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31.
- VDD:** Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31.
- VREF:** Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31.
- Control Signals:**
 - DQ32-DQ39:** Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31.
 - DQ40-DQ47:** Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31.



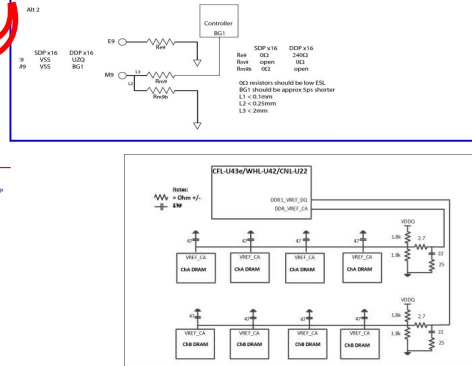
Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed, R2 = 0 ohms

Note: B01 + B02 + M should be 25ms shorter than other CMD signals.



- ▶ Alternate two layout, risk of VSS offset increases a little



The image displays a detailed PCB layout for power planes and decoupling capacitors. The layout is organized into several horizontal sections, each representing a different power supply:

- VDDQ/VDD 10uF x6:** The top section shows a horizontal bus with six 10uF capacitors (C1305, C1306, C1307, C1308, C1309, C1310) connected to a common rail. A red circle highlights a specific capacitor (C1307) labeled "DY".
- VDDQ/VDD 1uF x20:** The second section shows a horizontal bus with twenty 1uF capacitors (C1313 through C1332) connected to a common rail. A red circle highlights a specific capacitor (C1317) labeled "CHA".
- VPP 10uF x4:** The third section shows a horizontal bus with four 10uF capacitors (C1323 through C1326) connected to a common rail. A red circle highlights a specific capacitor (C1324) labeled "DY".
- VTT 10uF x2:** The bottom section shows a horizontal bus with two 10uF capacitors (C1347, C1348) connected to a common rail. A red circle highlights a specific capacitor (C1347) labeled "CHA".

The layout also includes various other components and labels, such as "CHA", "DY", "VDDQ", "VDD", "VPP", "VTT", and "GND". The capacitors are connected to a common rail, and the layout is designed to ensure proper power distribution and decoupling across the board.

Memory Configuration	Power Domain	Decoupling Location	Qty x μF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible distribute evenly across domain, close by Drams	32x 1 μF (0402) (All stuffed) 10x 10 μF (0603) (All stuffed)
	VPP	2 per dram, as close as possible distribute evenly across domain, close by Drams	16x 1 μF (0402) 5x 10 μF (0603)
	VTT	distributed along termination resistors distribute evenly across domain	16x 1 μF (0402) 4x 10 μF (0603)

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DDR (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

Rev
-1M

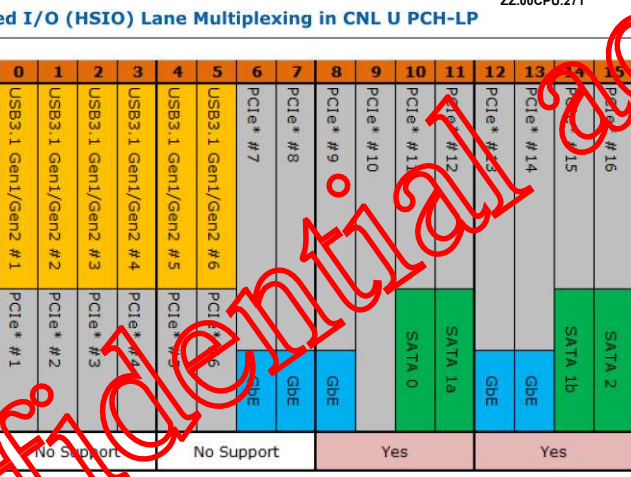
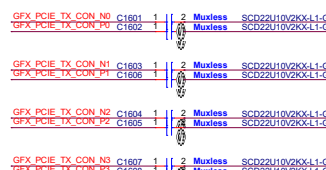
Date: Tuesday, September 25, 2018

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Description	XTAL Frequency Select	M.2 Pin Mode Select	3.0V Select	Reserved	eSPI Flash Sharing Mode
GPIO	GPP_H21	GPP_H22	MDIO_PSEL	GPD7	GPP_H23
Schematics					

[illegible]

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PCIe-LF		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
Flex I/O Lane		0	1	2	3	4	5	6	7	Cycle Router #2				Cycle Router #3			
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1	RP3			RP5	RP7			RP9	RP11			RP13	RP15		
	1x2+2x1	RP1	RP3	RP4		RP5	RP7	RP8	RP9	RP11	RP12	RP13	RP15	RP16			
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5	RP12	RP11	RP9	RP16	RP15	RP13			
4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	

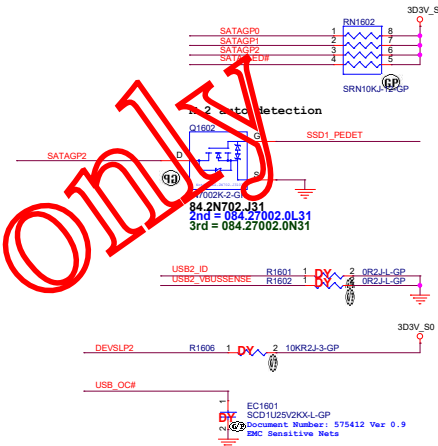
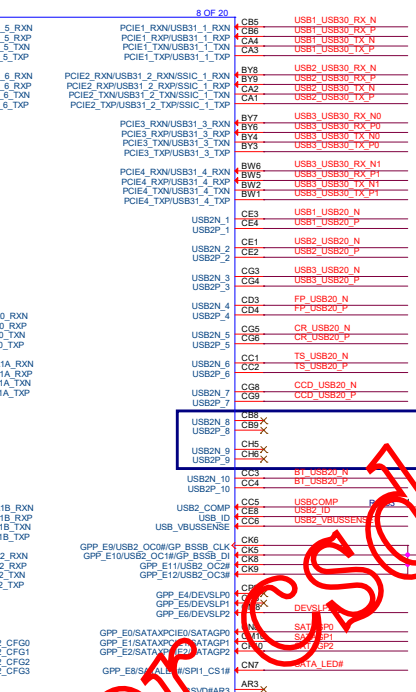


Figure 6-6. PCH PCIE_RCOMP and PCIE_RCOMP_N Connections

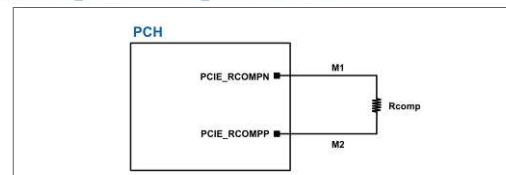


Table 6-10. PCH PCI Express* Compensation Routing Guidelines

Parameter	Segment	Stack-up (W/S, S/L, S/L)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	M1, M2	MS/SL/DSL	NA	GND	GND	GND
Series Resistor	M1, M2	MS	Ohms	100 +/- 1%	100 +/- 1%	100 +/- 1%
Motherboard Max Via Count	M1, M2	NA	vias	2	2	2
Motherboard Length Matching	M1, M2	MS/SL/DSL	mm(mils)	M1- M2 = $\pm 0.127\text{mm}$ ($\pm 5\text{mils}$)		

Notes:

1. Recommended placing a VSS shield of at least 4mils (0.1016mm) wide between the RCOMP signals and any adjacent I/O signals.
2. Avoid routing close to any clocks
3. Micro-Vias within the breakout area are not counted against maximum via total
4. Must maintain low DC resistance routing (<0.1 ohm)

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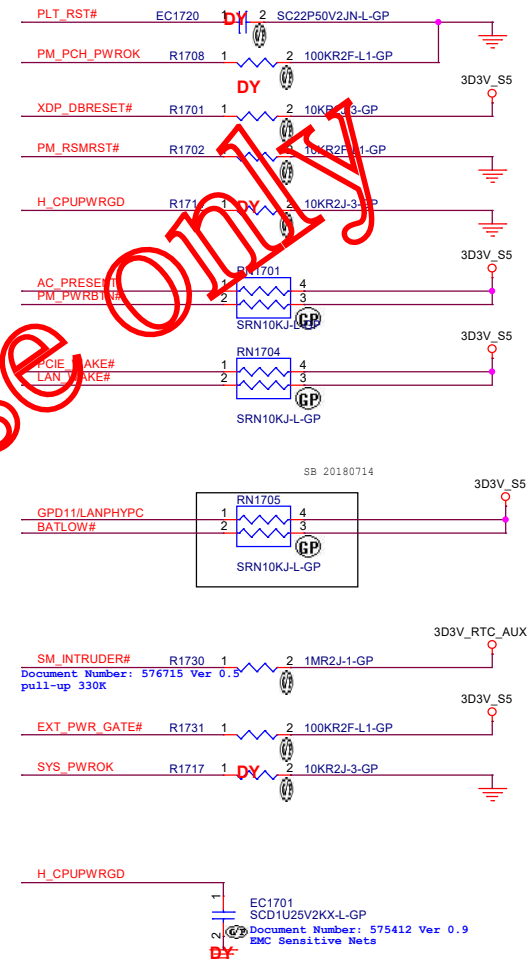
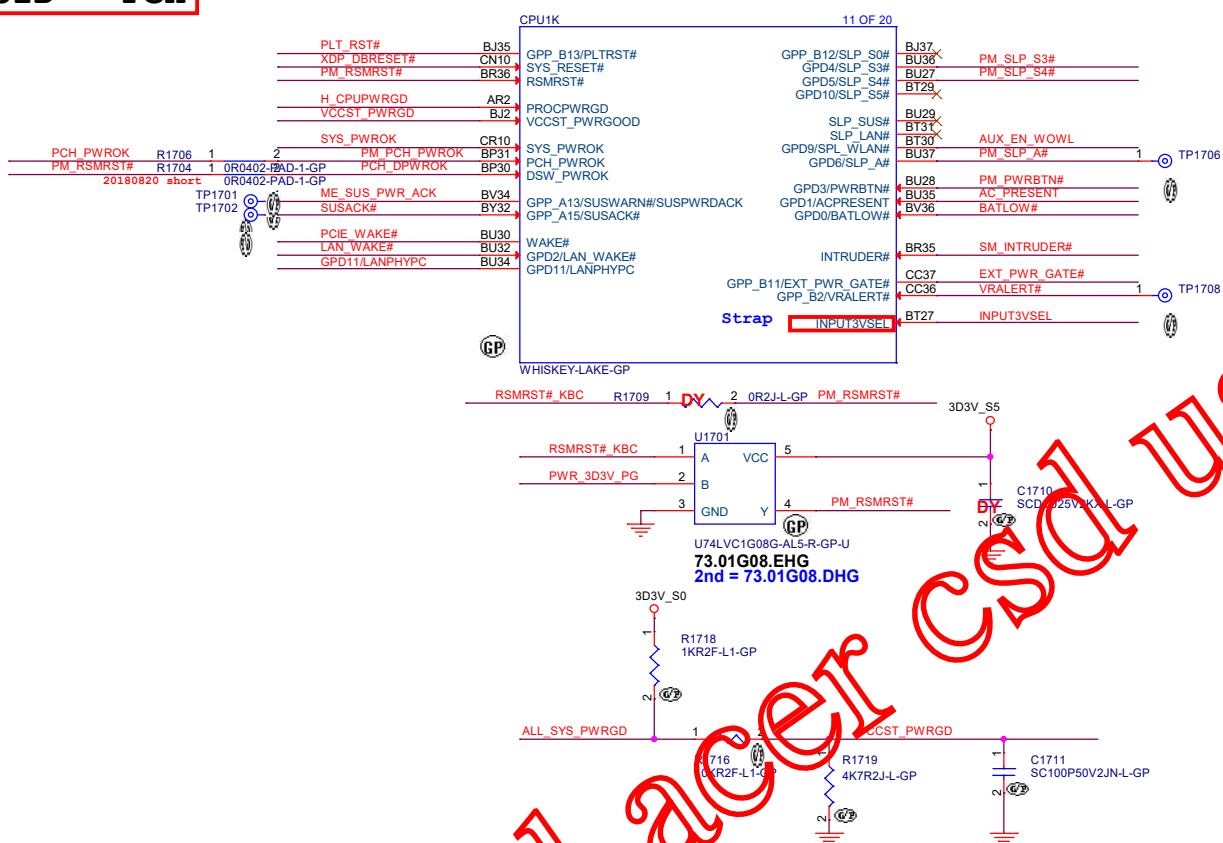
CNVi:

Bluetooth USB host bus (positive) for standard CNV. Optional to connect to a Bluetooth USB+ pin on the Bluetooth module. Port 10 is the recommended port but other USB2 ports can be selected for this function.

Document Number: 566439 Ver 2.0

SSID = PCH

24,31,61,63,68,79,89,91 PLT_RST# <<<
>>>
24 RSMRST#_KBC >>>
45,53 PWR_3D3V_PG >>>
24,40 ALL_SYS_PWRGD >>>
24 SYS_PWROK >>>
40 PCH_PWROK >>>
31,61,63,89 PCIE_WAKE# <<<
>>>
24,40,58 PM_SLP_S3# <<<
24,40,51 PM_SLP_S4# <<<
24 PM_PWRBTN# >>>
24 AC_PRESENT >>>
15 INPUT3VSEL >>>
61 AUX_EN_WOWL <<<
>>>



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Title CPU (PMU)

Size A3 Document Number Raichu_WL/Pikachu_WL Rev -1M

Date: Monday, October 01, 2018 Sheet 17 of 106

SSID = PCH

24.25.91 SPI_CLK_CPU1
24.25.91 SPI_SD_CPU1
24.25.91 SPI_SI_CPU1
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24.25 SPI_CS_CPU_N0

15 SPI_SI_CPU
15 SPI_WP_CPU
15 SPI_HOLD_CPU

29 DMIC2_DET#
24 H_RCIN#
24.68 INT_SERIRQ
13 SMB_DATA_CPU
13 SMB_CLK_CPU

24.79 SML1_CLK
24.79 SML1_DATA

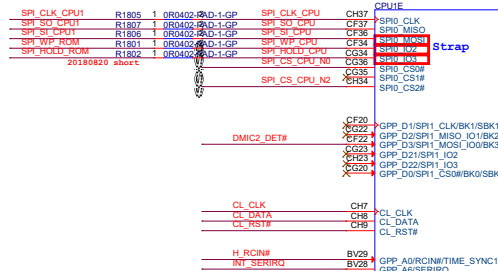
15 GPP_C2/SMBALERT#
15 GPP_C5/SMLALERT#
15 GPP_B23/SML1ALERT#

24.68 LPC_AD_CPU_P0
24.68 LPC_AD_CPU_P1
24.68 LPC_AD_CPU_P2
24.68 LPC_AD_CPU_P3
24.68 LPC_FRAME#_CPU

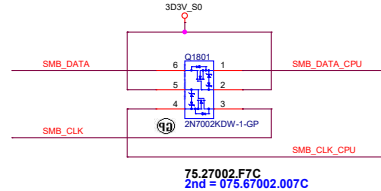
24 LPC_CLK_KBC
68.89 LPC_CLK_DBG

24 PM_CLKRUN#_EC
91 SPI_CS_CPU_N2

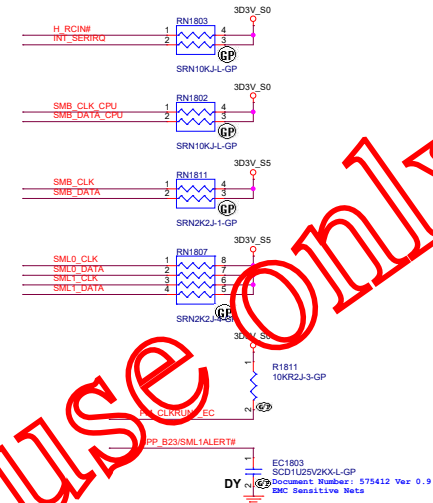
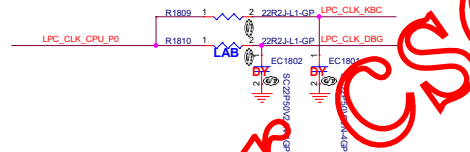
61 CL_CLK
61 CL_DATA
61 CL_RST#



ZZ.00CPU.271



75.27002.F7C
2nd = 075.67002.007C



76 PEG_CLK_CPU_N
76 PEG_CLK_CPU_P
76 PEG_CLKREQ_CPU#

61.89 WLAN_CLK_CPU_N
61.89 WLAN_CLK_CPU_P
61.89 WLAN_CLKREQ_CPU#

63 SSD1_CLK_CPU_N
63 SSD1_CLK_CPU_P
63 SSD1_CLKREQ_CPU#

24 RTCRST_ON

31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU#

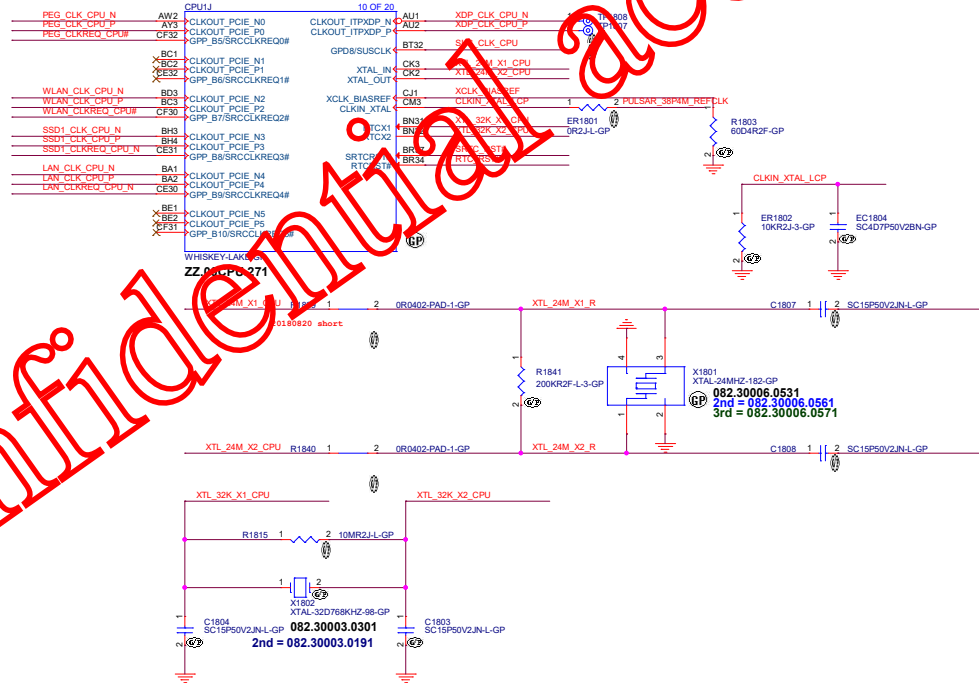
61 PULSAR_38PM_REFCLK
61 SUS_CLK_CPU

DIS

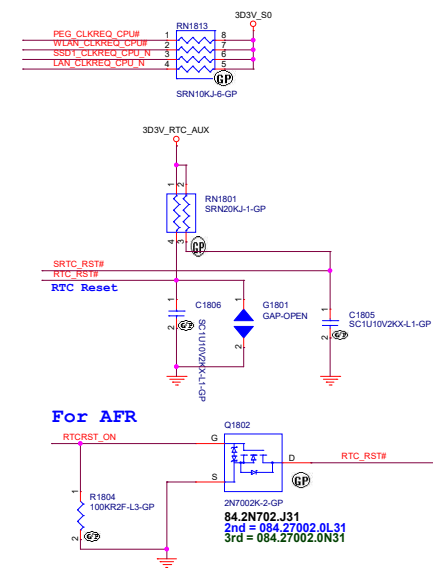
WLAN

SSD

LAN



ZZ.00CPU.271



For AFR

84.2N702.J31
2nd = 084.27002.01.31
3rd = 084.27002.0N31

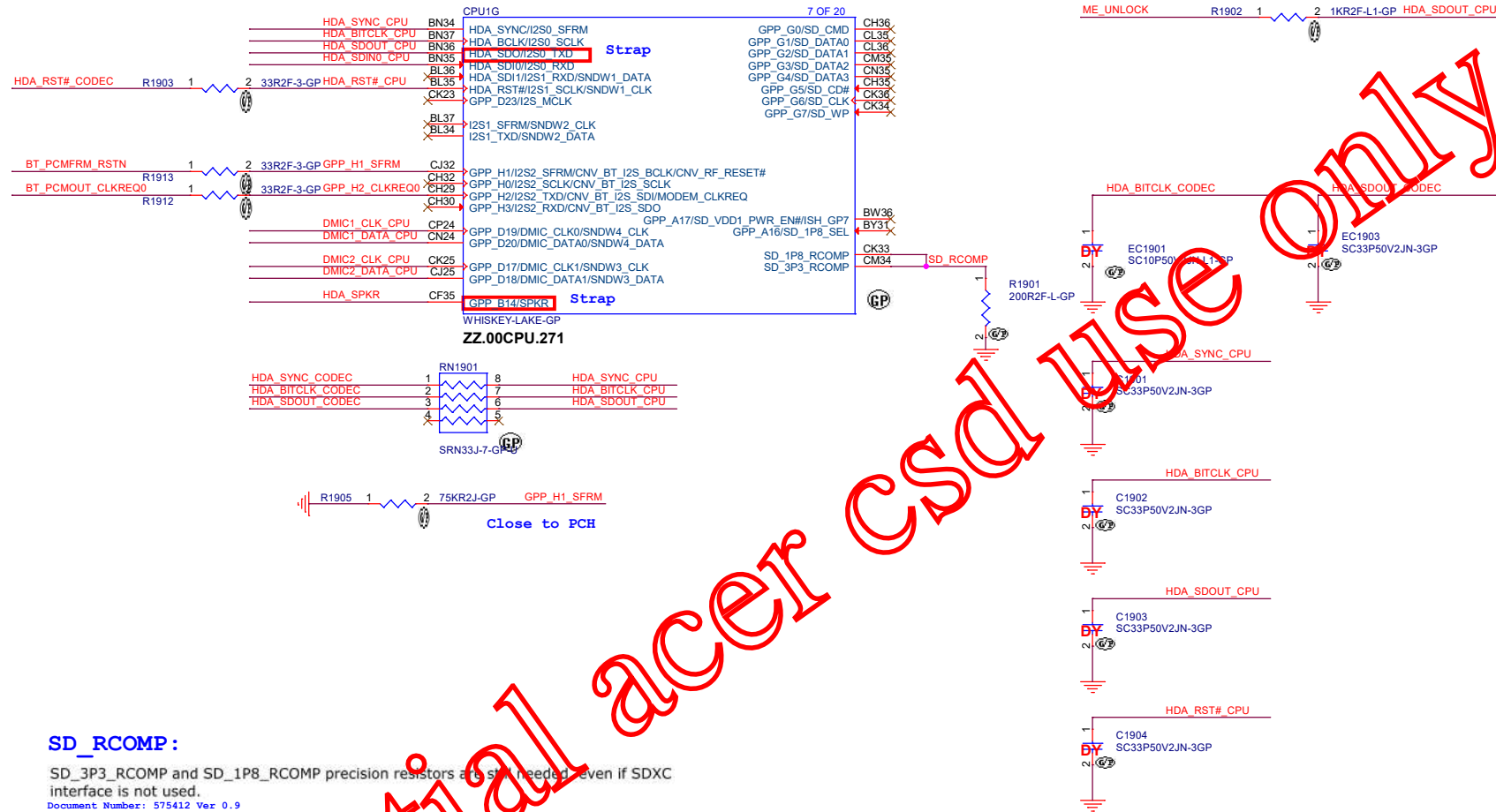
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title CPU(SPI/ESPI/SMB/XTAL/CLK)
Rev 1.0
Document Number Raichu_WL/Pikachu_WL-1M
Date: Tuesday, October 02, 2018 Sheet 18 of 108

SSID = PCH

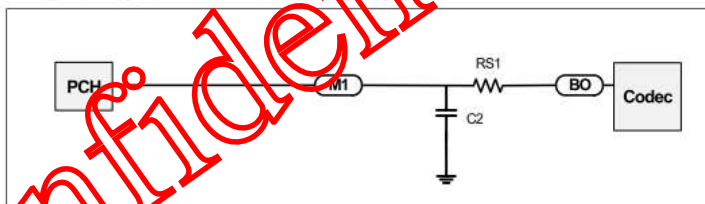
- 27 HDA_SYNC_CODEC <<
- 27 HDA_BITCLK_CODEC <<
- 15 HDA_SDOUT_CPU >>
- 27 HDA_SDOUT_CODEC <<
- 24 ME_UNLOCK <<
- 27 HDA_SDI0_CPU >>
- 27 HDA_RST#_CODEC <<
- 55 DMIC1_CLK_CPU >>
- 55 DMIC1_DATA_CPU >>
- 29 DMIC2_CLK_CPU >>
- 29 DMIC2_DATA_CPU >>
- 15,27 HDA_SPKR <<
- 61 BT_PCMOUT_CLKREQ0 >>>
- 61 BT_PCMFRM_RSTN <<<



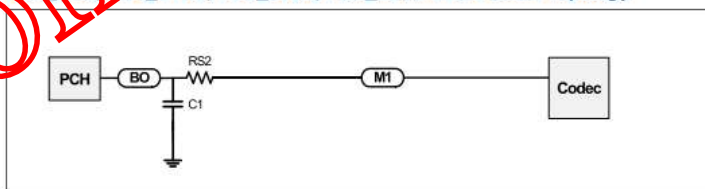
SD_RCOMP:

SD_3P3_RCOMP and SD_1P8_RCOMP precision resistors are still needed even if SDXC interface is not used.
Document Number: 575412 Ver 0.9

HDA_SDI Single Load Audio Down Topology



HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Topology



Document Number: 575412 Ver 0.9

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Title			CPU (HDA/I2S/SD/DMIC)	
Size	Document Number	Raichu_WL/Pikachu_WL		Rev
A3				-1M
Date:	Tuesday, September 25, 2018	Sheet	19	of 106

SSID = PCH

Touch Pad

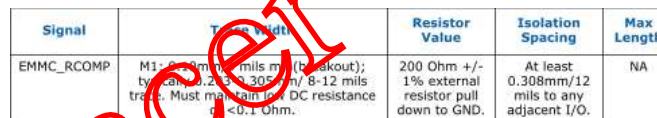
MEMORYID4	MEMORYID3	MEMORYID2	MEMORYID1	Supplier	Density	P/N	vendor P/N	
GPP_A19	GPP_A18	GPP_A21	GPP_A20					
0	0	0	0	HYNIX	8G	KN.8GB0G.049	H5AN8G6NAFR-UHC	SDP
0	0	0	1	Micron	8G	KN.8GB04.027	MT40A512M16LY-075:E	SDP
0	0	1	0	HYNIX	8G	KN.8GB0G.061	H5AN8G6NCJR-VKC	SDP
0	0	1	1	NA	NA	NA	DUMMY	NA

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Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (UART/I2C/ISH)
Size Custom Document Number Raichu_WL/Pikachu_WL Rev -1M
Date Tuesday, September 25, 2018 Sheet 20 of 106

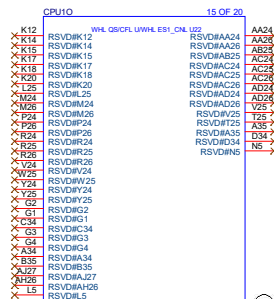
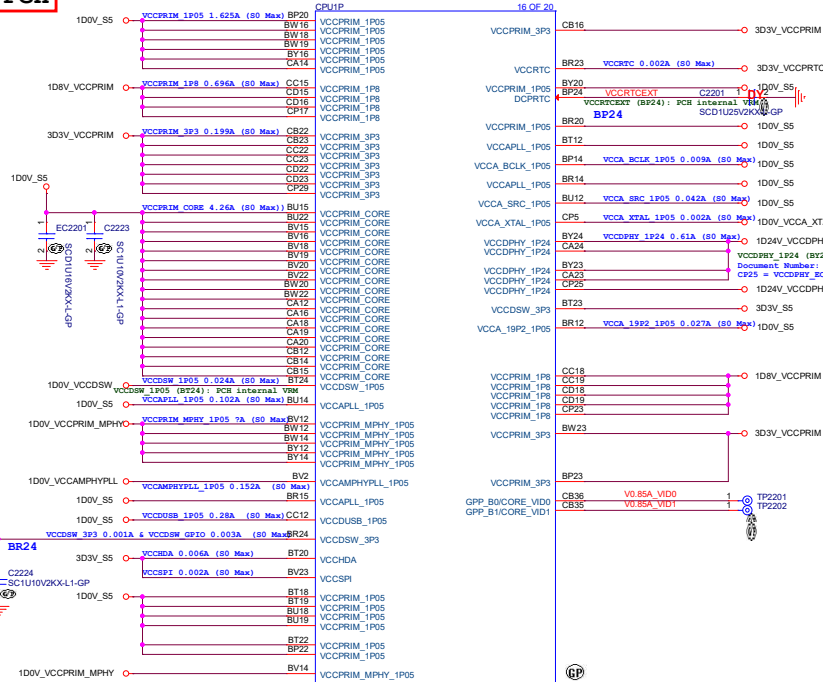
Document Number: 566439 Ver.2.0



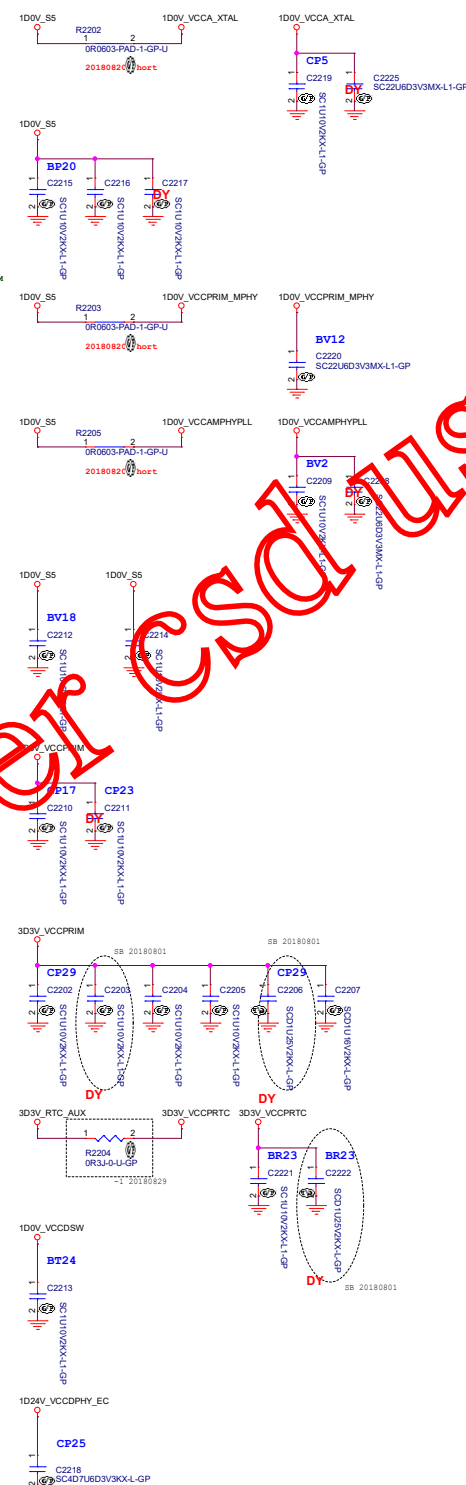
Document Number: 575412 ver. 0.9

Title				CPU (EMMC/CNVi)			
Size	Document Number					Rev	
A3	Raichu_WL/Pikachu_WL					-1M	
Date:	Tuesday, September 25, 2018		Sheet	21	of	106	

SSID = PCH



ZZ.00CPU.271

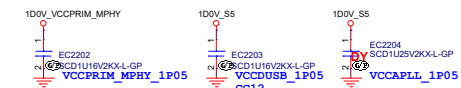


Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/J edge)	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC2	-	-	-	-	-
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, CP22, CP20, CP19, BW18, BW19, BW20, CA12, BY20, BU14, BT19, BU14, BT12	1uF	0508	1	E	BP20
	VCCMPHYGTG_1P05	BW14, BW12, BW14, BY12, BY14, BV14	22uF	0603	1	E	BV12
	VCC3.3V_1P05	BV2	1uF	0402	1	E	BV2
	VCCPRIM_COR_E	BU15, BU22, BV15, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CD12, CD14, CB18	1uF	0402	1	E	BV18, Note 1
	V1.05A / V0.1W						
Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/J edge)	Place capacitor(s) near ball(s)
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23, CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1
V3.3A	VCCPRIM_3P3	CB23, CB23, CC22, CD23, CP28, BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A / V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A / V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DS W	VCCDSW_GPTIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BP23, CA23, CP23, BV24, CA24	4.7uF	0402	1	E	CP25

Supply	Value	Quantity	Type	Notes
VCCA_XTAL_IPOS (Pin CPG) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	XSXR rating capacitor recommended
VCCAMPHYPLL_IPOS (Pin BV2) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	XSXR rating capacitor recommended

Document Number: 566439 Ver 2.0

Document Number: 575412 Ver 0.9
EMC Sensitive Nets



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Title	CPU (PCH-LP PWR&Caps)
-------	----------------------------------

Size A2	Document Number Raichu_WL/Pikachu_WL	Rev -1
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SSID = PCH

CPU1R 18 OF 20	
CR34	VSS
BT5	VSS
BY5	VSS
CP35	VSS
CM37	VSS
CK37	VSS
AW11	VSS
CM11	VSS
BD6	VSS
AY4	VSS
B34	VSS
E35	VSS
A4	VSS
AE24	VSS
AE26	VSS
AF25	VSS
AG24	VSS
AG26	VSS
AH24	VSS
AH25	VSS
B2	VSS
B36	VSS
C36	VSS
C37	VSS
CN1	VSS
CN2	VSS
CN37	VSS
CP2	VSS
D1	VSS
A32	VSS
F33	VSS
A3	VSS
BJ7	VSS
CJ36	VSS
A36	VSS
BK10	VSS
CJ4	VSS
AB27	VSS
BK2	VSS
CK1	VSS
AB3	VSS
BK28	VSS
AB30	VSS
BK3	VSS
CK4	VSS
AB33	VSS
BK33	VSS
CK7	VSS
AB36	VSS
BK4	VSS
CL2	VSS
AB4	VSS
BK7	VSS
CM13	VSS
AB7	VSS
BL25	VSS
CM17	VSS
AC10	VSS
BL28	VSS
CM21	VSS
AC27	VSS
BL29	VSS
CM25	VSS
AC30	VSS
BL30	VSS
CM29	VSS
BL31	VSS
CM31	VSS
AD33	VSS
BL32	VSS
CM33	VSS
AD35	VSS

GP WHISKEY-LAKE-GP

CPU1S 19 OF 20	
BT35	VSS
D6	VSS
AL32	VSS
BT36	VSS
D8	VSS
AE27	VSS
AL7	VSS
D9	VSS
AM10	VSS
BU11	VSS
E23	VSS
AM28	VSS
E27	VSS
BM9	VSS
AM33	VSS
BU23	VSS
E29	VSS
AM35	VSS
BU24	VSS
E31	VSS
BU25	VSS
E33	VSS
AN25	VSS
AN25	VSS
BU7	VSS
E9	VSS
AN28	VSS
AF36	VSS
F12	VSS
CN5	VSS
AF7	VSS
F15	VSS
AN30	VSS
F18	VSS
AN31	VSS
BV3	VSS
F2	VSS
AN7	VSS
CP11	VSS
BV31	VSS
F21	VSS
AN8	VSS
BV33	VSS
F24	VSS
BV4	VSS
F3	VSS
AP3	VSS
AP3	VSS
BW11	VSS
F4	VSS
AP33	VSS
BW15	VSS
G21	VSS
AP36	VSS
G27	VSS
AP4	VSS
G33	VSS
AR28	VSS
G35	VSS
GA25	VSS
AT33	VSS
BW24	VSS
G9	VSS
AT35	VSS
H21	VSS
AT36	VSS
BW7	VSS
H27	VSS
AT	VSS
BY	VSS
AU	VSS
BY15	VSS
D25	VSS
AK4	VSS
BT28	VSS
AL28	VSS
BT33	VSS
D5	VSS
AL29	VSS

GP WHISKEY-LAKE-GP

CPU1T 20 OF 20	
N6	VSS
B37	VSS
CB3	VSS
P10	VSS
B5	VSS
CB33	VSS
J24	VSS
B7	VSS
CB4	VSS
P33	VSS
B9	VSS
CB7	VSS
P36	VSS
BA10	VSS
CC11	VSS
P4	VSS
BA28	VSS
P7	VSS
BA3	VSS
CC20	VSS
R27	VSS
BB3	VSS
CC25	VSS
R28	VSS
BB33	VSS
CC28	VSS
R29	VSS
BB36	VSS
CC31	VSS
R30	VSS
BB4	VSS
CC7	VSS
R31	VSS
BC25	VSS
CD11	VSS
R27	VSS
CD12	VSS
R30	VSS
CD14	VSS
R35	VSS
BC32	VSS
CD24	VSS
K31	VSS
CD25	VSS
T7	VSS
CE33	VSS
U26	VSS
BD28	VSS
CE35	VSS
U7	VSS
BD33	VSS
CE36	VSS
V26	VSS
BD35	VSS
CE7	VSS
V27	VSS
BD36	VSS
CF11	VSS
V3	VSS
BE10	VSS
CF14	VSS
V30	VSS
BE28	VSS
CF19	VSS
V33	VSS
BE29	VSS
CF2	VSS
V36	VSS
BE3	VSS

GP WHISKEY-LAKE-GP

<Core Design>

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Title CPU (VSS)

Size A3 Document Number Raichu_WL/Pikachu_WL Rev -1M

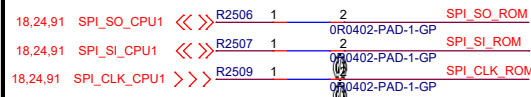
Date: Tuesday, September 25, 2018 Sheet 23 of 106


```

18,24 SPI_CS_CPU_N0    >>>_____
      18 SPI_WP_ROM    <<>>_____
      18 SPI_HOLD_ROM  <<>>_____
      20 RTC_DET#      <<<_____

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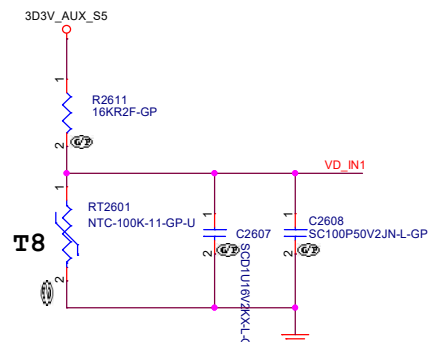
SPI ROM Equal length need to less than 500mil

[illegible]

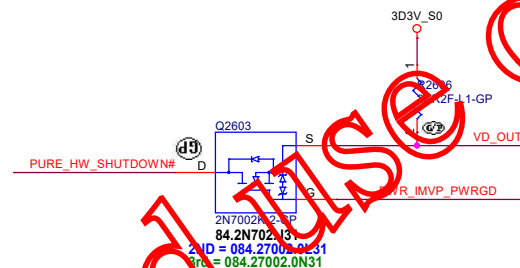
2nd=023.22032.0611

Title				Flash/RTC			
Size	Document Number	Rev					
Custom	Raichu_WL/Pikachu_WL	-1M					
Date:	Tuesday, September 25, 2018		Sheet	25	of	106	

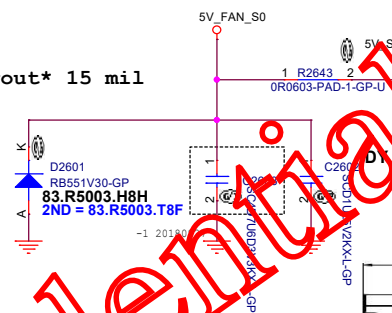
SSID = Thermal



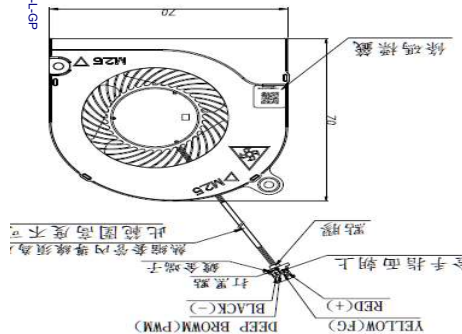
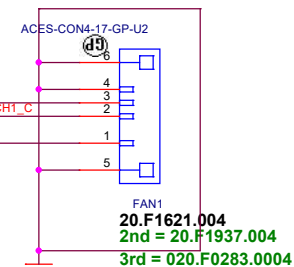
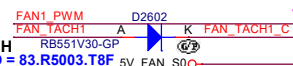
RT2601 close CPU and Vcore chock
VD_IN1 trace 10 mli



Layout 15 mil



83.R5003.H8H
2ND = 83.R5003.T8F



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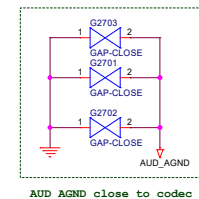
<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title Thermal 7718/Fan Controllor P2793</p>	
Size Custom	Document Number Raichu WL/Pikachu WL
Date: Tuesday, September 25, 2018	Sheet 26 of 106

```

19  HDA_BITCLK_CODEC <<<
19  HDA_SYNC_CODEC <<<
19  HDA_SDBUS_CPU <<<
19  HDA_SSCUT_CODEC <<<
19  HDA_RSTB_CODEC <<<—

      24 AMP_MUTE#
29,55 DMIC2_DATA_CON
29,55 DMIC_CLK_CON
55 DMIC2_DATA_CON
29 AUD_HPI1 JACK_L2
29 AUD_HPI1 JACK_R2
29,89 AUD_HPI1_IDE
29,89 RING2
29,89 SELEVEE
24 KBC BEEP
15,19 HDA_SPKR
89 AUD_SPK1_R_L+
89 AUD_SPK1_R_L-
89 AUD_SPK1_R_R+
89 AUD_SPK1_R_R-

```



I_{omax}=120mA

Fix $V_{out}=1.5V$
 $I_{max}=300mA$
 $OCP = 400mA$

Layout Not

Far field:ALC256M(071.00256.0003)
No far field:ALC255(071.00255.0003)

0 071.00256.0003

Vinafix

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Title		Audio Codec ALC256		Rev
Size	Document Number	Raichu WL/Pikachu WL		-1
Custom				
Date:	Monday, October 01, 2018	Sheet	27	of 106

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Title

Audio (RSVD)

Size
A4

Document Number

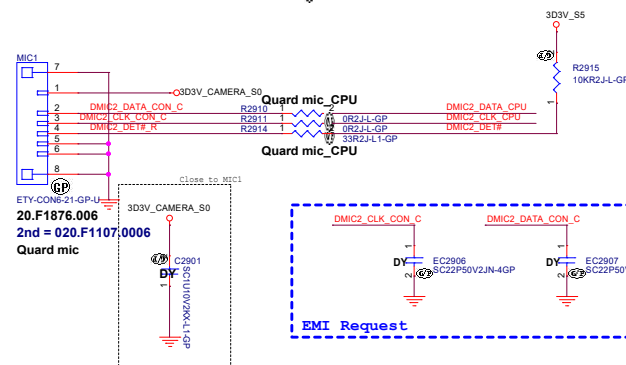
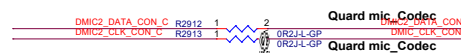
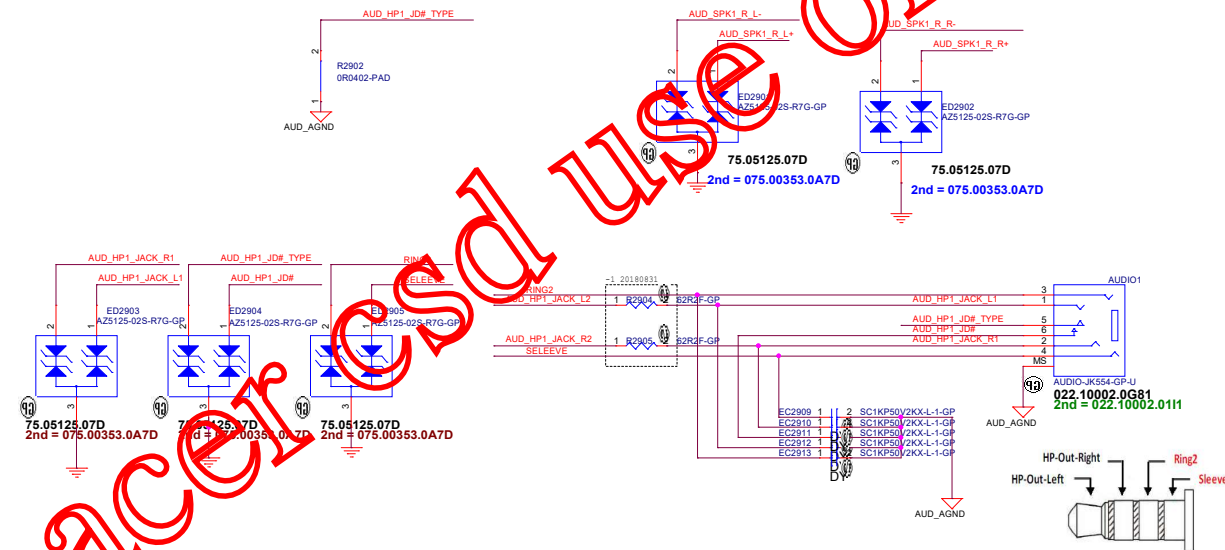
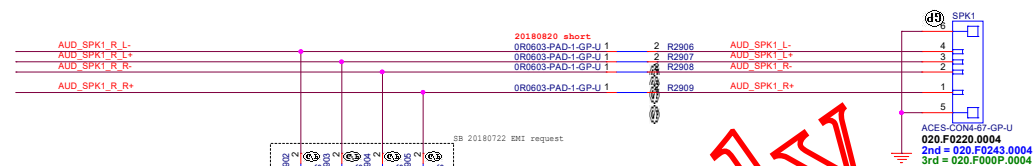
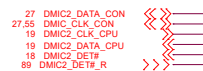
Raichu_WL/Pikachu_WL

Rev
-1M

Date: Tuesday, September 25, 2018

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Speaker



緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Speaker/HPMIC**

Number	Rev
Raichu WL/Pikachu WL	-1M
Number 25, 2018	Sheet 29 of 106

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Title

Audio (RSVD)

Size
A4

Document Number

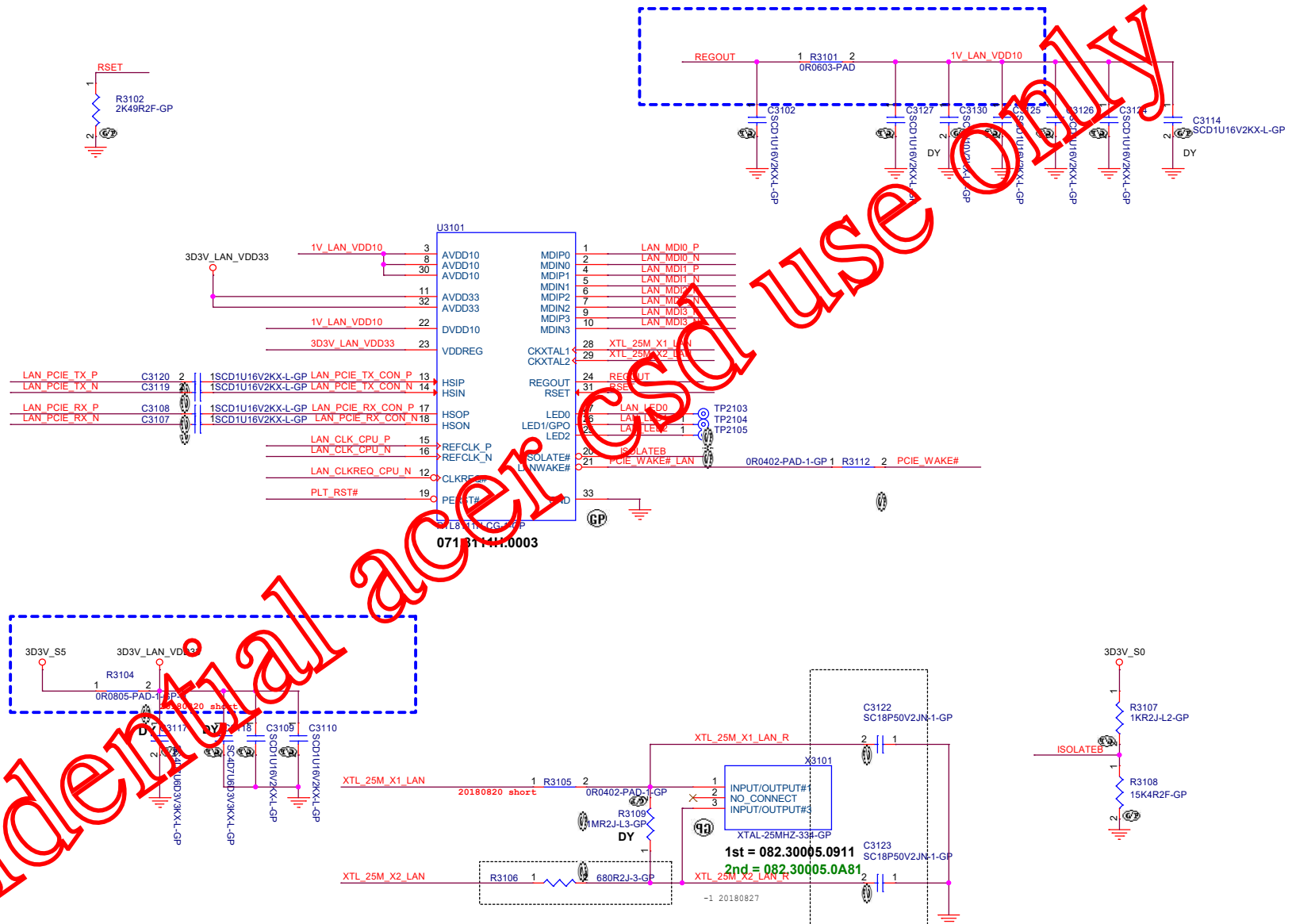
Raichu_WL/Pikachu_WL

Rev
-1M

Date: Tuesday, September 25, 2018

Sheet 30 of 106

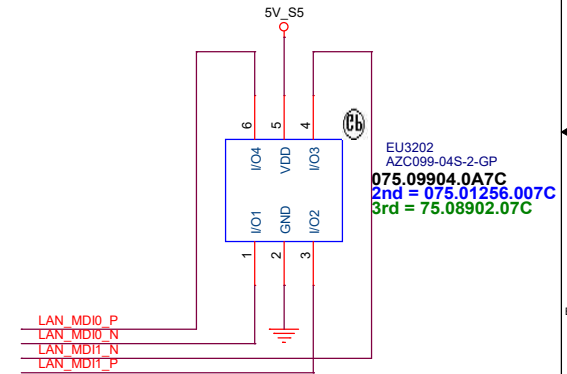
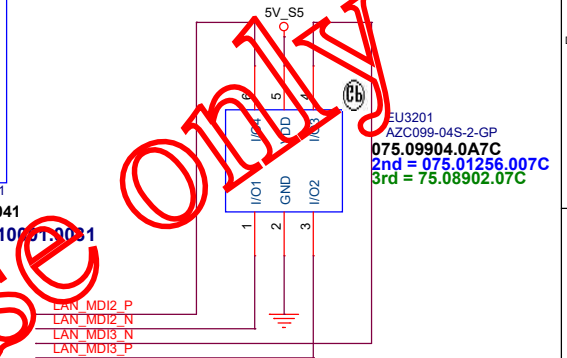
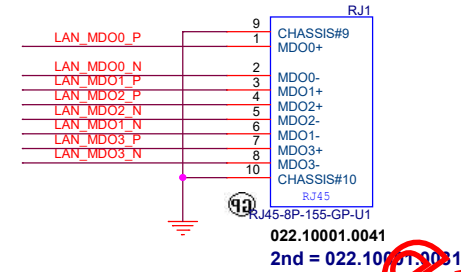
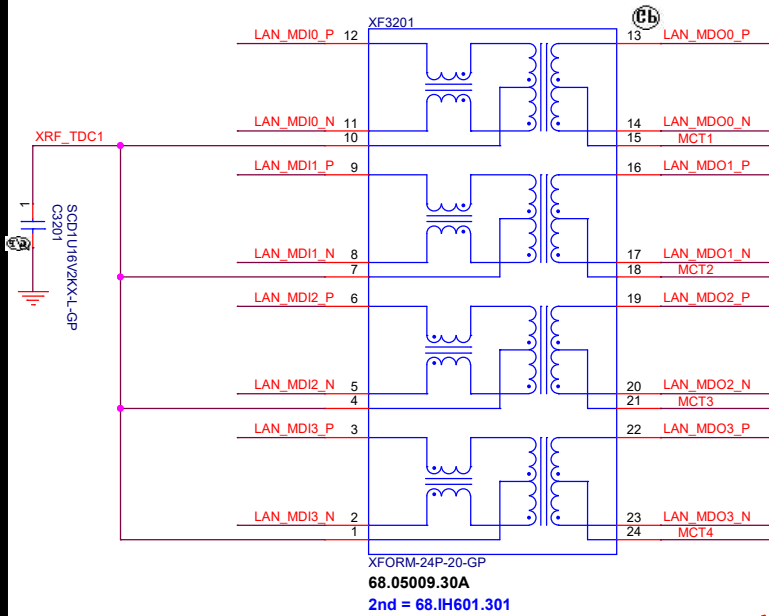
16 LAN_PCIE_TX_P >>>
 16 LAN_PCIE_TX_N >>>
 16 LAN_PCIE_RX_P >>>
 16 LAN_PCIE_RX_N >>>
 18 LAN_CLK_CPU_P >>>
 18 LAN_CLK_CPU_N >>>
 18 LAN_CLKREQ_CPU_N <<<
 17,24,61,63,68,79,89,91 PLT_RST# >>>
 17,61,63,89 PCIE_WAKE# <<<
 32 LAN_MDI0_P >>>
 32 LAN_MDI0_N >>>
 32 LAN_MDI1_P >>>
 32 LAN_MDI1_N >>>
 32 LAN_MDI2_P >>>
 32 LAN_MDI2_N >>>
 32 LAN_MDI3_P >>>
 32 LAN_MDI3_N >>>



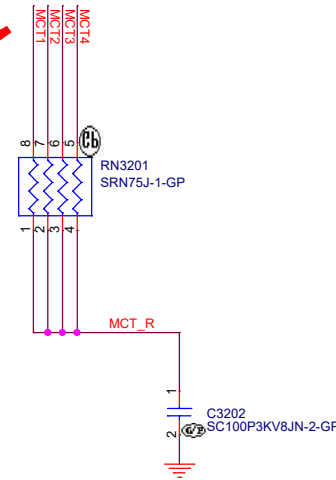
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN(RTL8111H)	
Size A3	Document Number Raichu WL/Pikachu WL
Date Tuesday, October 02, 2018	Rev -1M

SSID = LAN



31 LAN_MDI0_P
31 LAN_MDI0_N
31 LAN_MDI1_P
31 LAN_MDI1_N
31 LAN_MDI2_P
31 LAN_MDI2_N
31 LAN_MDI3_P
31 LAN_MDI3_N



<Core Design>

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Title RJ45+Transformer
Size B Document Number Rev
Raichu_WL/Pikachu_WL -1M
Date: Tuesday, September 25, 2018 Sheet 32 of 106

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Title

USB (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

Rev
-1M

Date: Tuesday, September 25, 2018

Sheet 34 of 106

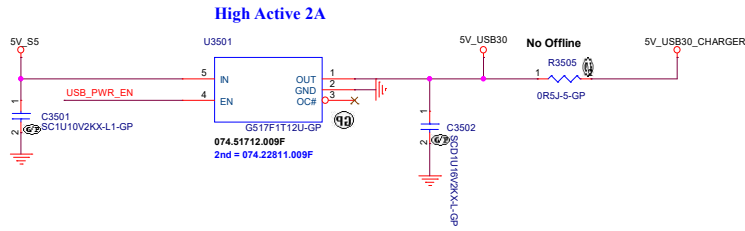
16 USB1_USB20_N <<>>
16 USB1_USB20_P <<>>
24 USB_PWR_EN >>>
16 USB1_USB30_RX_N <<>>
16 USB1_USB30_RX_P <<>>
16 USB1_USB30_TX_N <<>>
16 USB1_USB30_TX_P <<>>

89 USB1_CON_USB20_N <<>>
89 USB1_CON_USB20_P <<>>

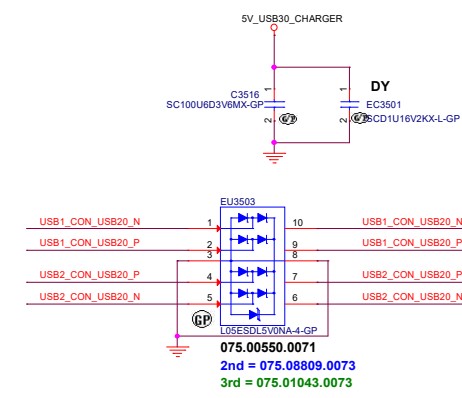
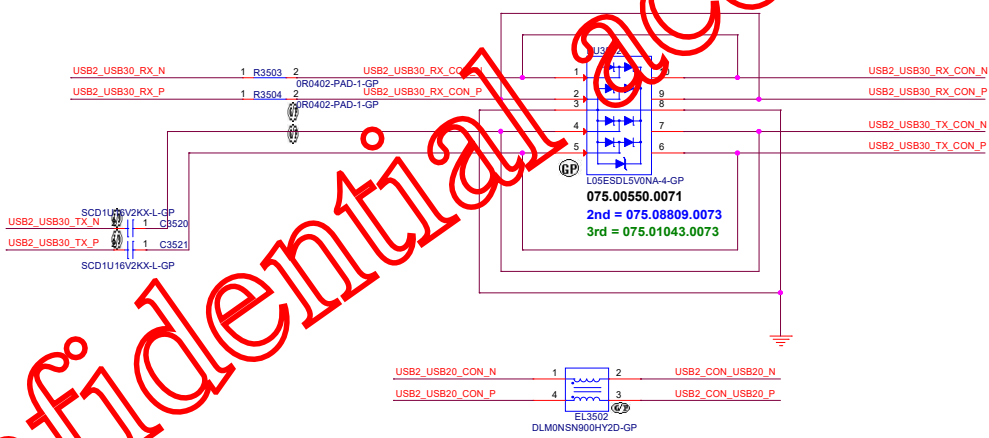
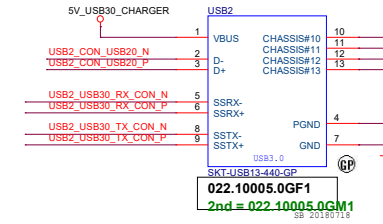
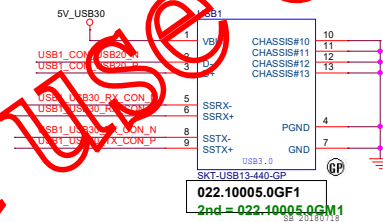
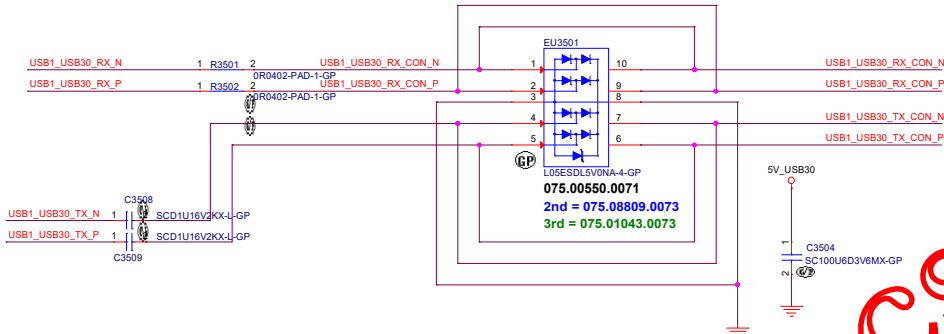
36 USB2_USB20_CON_N <<>>
36 USB2_USB20_CON_P <<>>

16 USB2_USB30_RX_N <<>>
16 USB2_USB30_RX_P <<>>
16 USB2_USB30_TX_N <<>>
16 USB2_USB30_TX_P <<>>

89 USB2_CON_USB20_N <<>>
89 USB2_CON_USB20_P <<>>



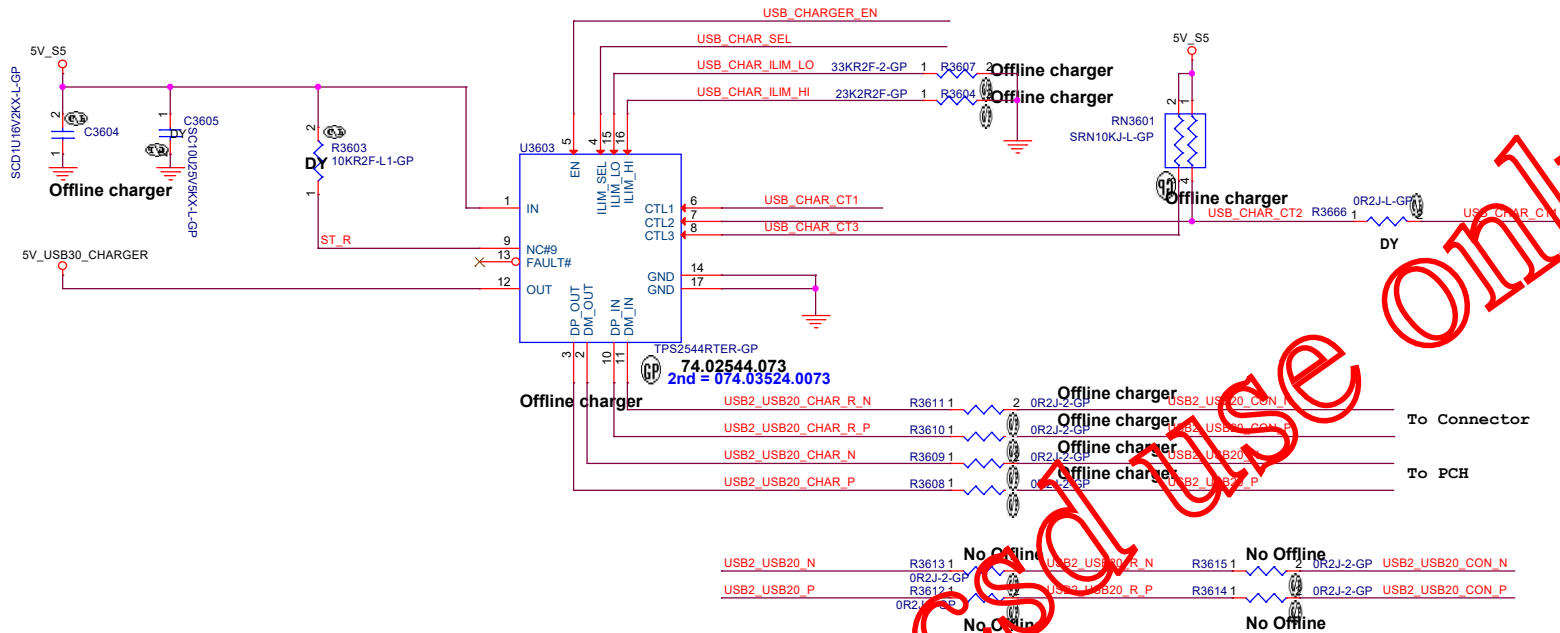
USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



24 USB_CHARGER_EN >>>
24 USB_CHAR_SEL >>>
24 USB_CHAR_CT1 >>>

To Connector
35 USB2_USB20_CON_N <<<
35 USB2_USB20_CON_P <<<

To PCH
16 USB2_USB20_N <<<
16 USB2_USB20_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP Auto	ILIM_HI	Data Lines
0	1	1	X			Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines
0	1	0	1		ILIM_HI	Connected
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP and 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines
1	1	0	1	SDP2	ILIM_HI	Connected
1	1	1	0	SDP3	ILIM_LO	Data Lines
1	1	1	1	DCP	ILIM_HI	Connected

S0 and S3 (at low battery and non support charger)

S0 and S5 state

S0 and S3 (at low battery and non support charger)

S0 state

<Core Design>	
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Title USB CHARGER	
Size Custom	Document Number Raichu_WL/Pikachu_WL
Date: Tuesday, September 25, 2018	Rev -1M
Sheet 36 of 106	

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Title

USB (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

Rev
-1M

Date: Tuesday, September 25, 2018

Sheet 37 of 106

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Title

USB (RSVD)

Size
A4

Document Number

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Rev
-1M

Date: Tuesday, September 25, 2018

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Title

Sequence (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

Rev
-1M

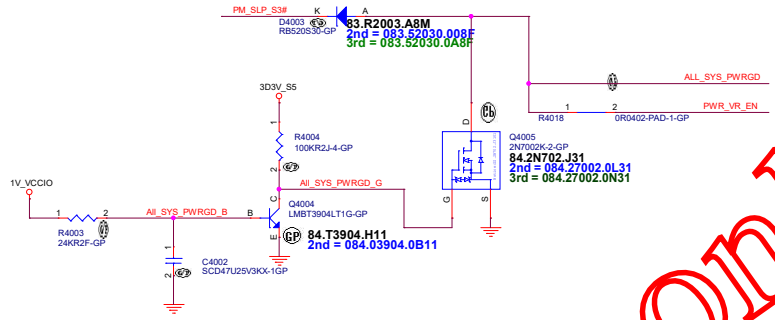
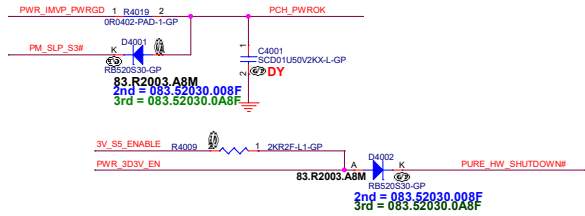
Date: Tuesday, September 25, 2018

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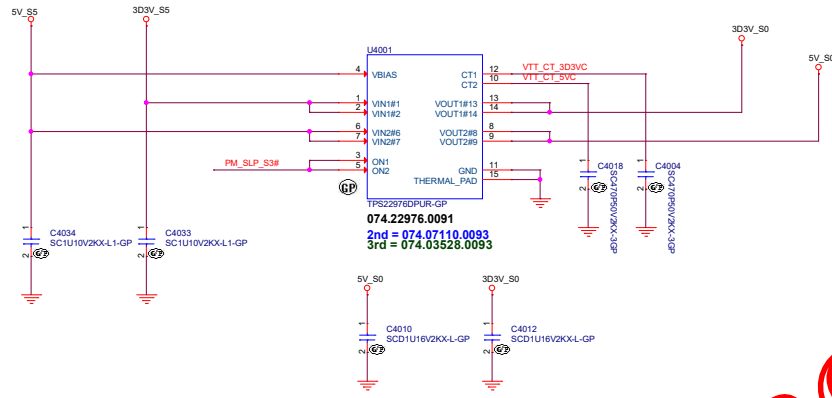
26,46 PWR_IMVP_PWRGD >>>
17,24,58 PM_SLP_S3# >>>
17 PCH_PWR0K <<<
24 3V_S5_ENABLE <<<
45 PWR_3D3V_EN <<<

24,26 PURE_HW_SHUTDOWN# >>>
17,24 ALL_SYS_PWRGD <<<
46 PWR_VR_EN <<<
17,24,51 PM_SLP_S4# >>>

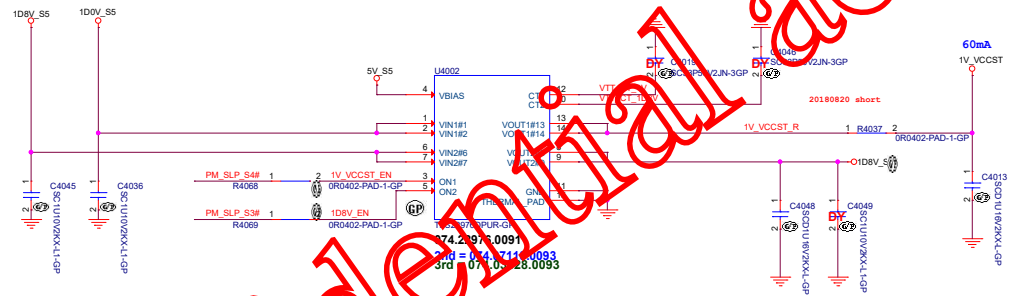
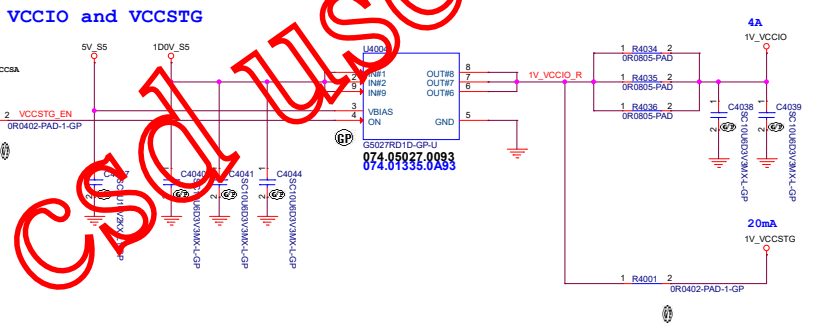
Power Sequence



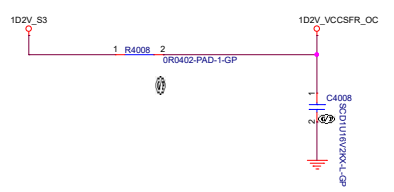
ANNIE Run Power



1126 Simon
Tuning RC for DRAM
VCCIO = SLP_S3
2.5v = SLP_S4
VCCIO effect VCCBA
Sequence should
Z004 =
SLP_S4 > 2.5V > VDDQ > VCCIO > VCCBA



VccPLL_OC



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Title

Sequence (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

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Date: Tuesday, September 25, 2018

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Title

INT IO (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

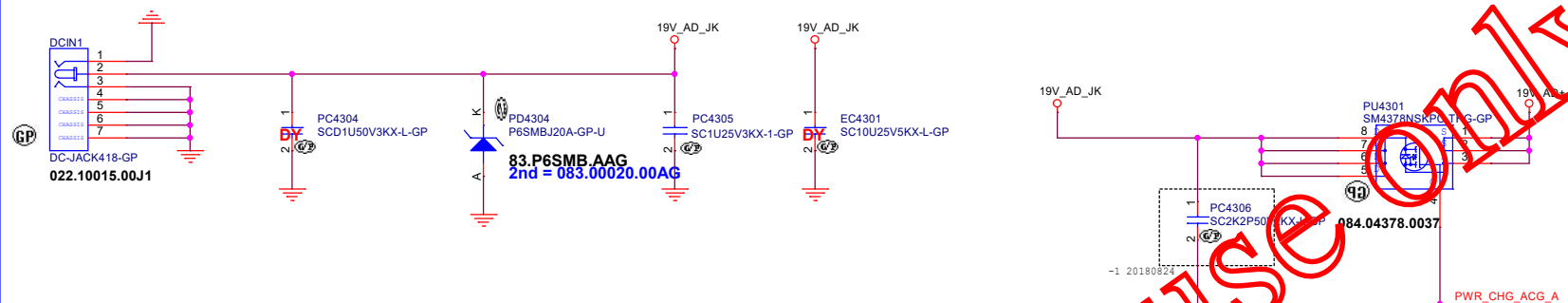
Rev
-1M

Date: Tuesday, September 25, 2018

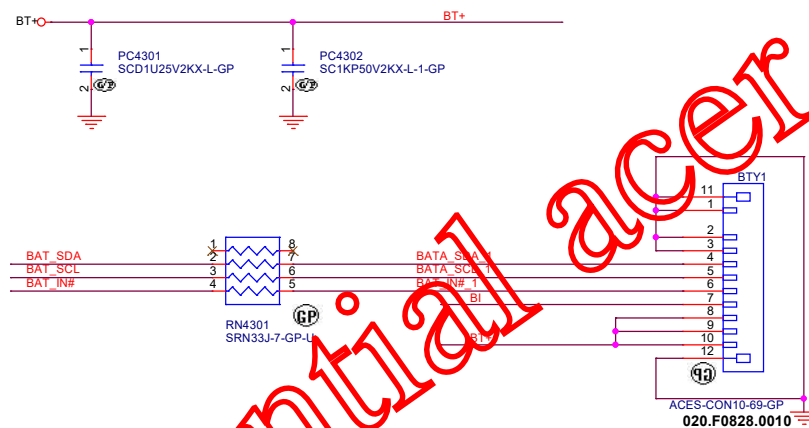
Sheet 42 of 106

ANNIE solution

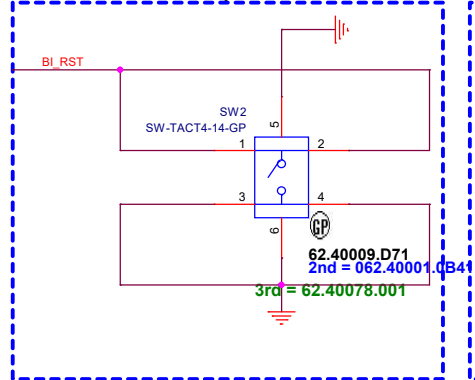
Adaptor in to generate DCBATOUT



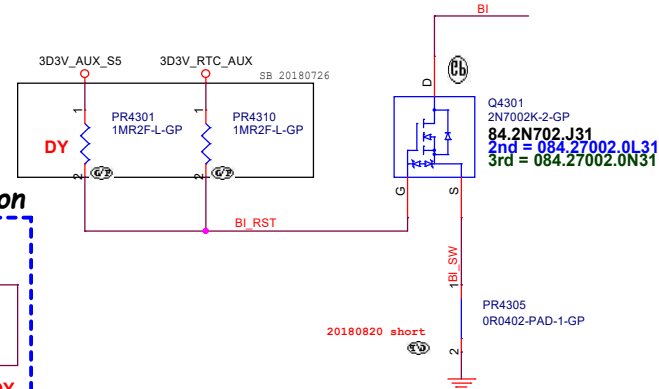
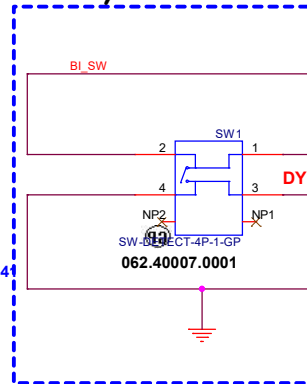
BATTERY CONNECTOR



Battery Reset Button



Battery Insert Button

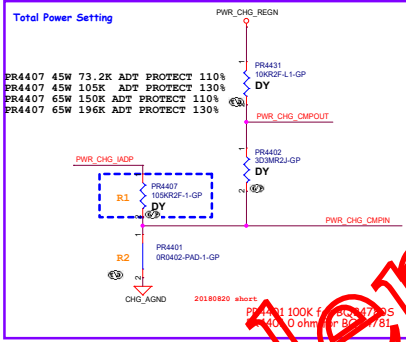
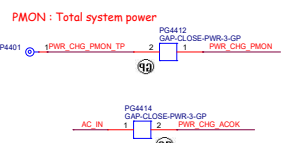
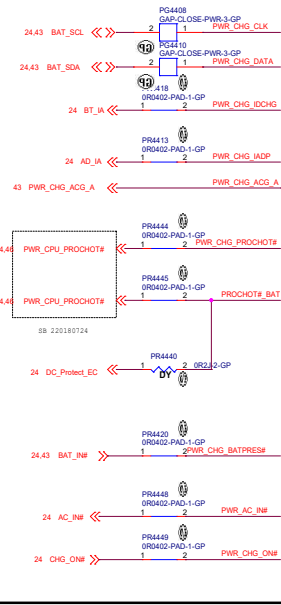


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Taipei Hsien 221, Taiwan, R.O.C.

INT IO (DC IN/BAT CON)			
Title	Size	Document Number	Rev
	A3	Raichu_WL/Pikachu_WL	-1M
Date: Tuesday, October 16, 2018	Sheet	43	of 106

SSID = Charger



IADP: AC adapter detect current
IADP: 20 or 40 x (Vacc - Vacn) / 100 ohm
IDCHG: Discharge detect current
= 8 or 16 x (Vsrn - Vsp)

PQ4408 1:1 for BQ24780S
PQ4408 DY for BQ24781

Sta	PM_SELF_A8	Adaptive Control	AC_Protect_percent	AC_Protect_Count	Stable status	IADP_GAIN	CM_VREF	Current to Voltage	PR4407	PR4408	CAL	Vcomp	Vsense	R1	R2
45W	AC+Battery	High	9.1	100%	2.4174	20	40	1.2V	1.93392	604	100	1.213598	1.7136	41.2	100
45W	AC+Battery	High	2.37	100%	2.4174	20	40	1.2V	1.93392	604	100	1.205686	1.93392	604	100
65W	AC+Battery	High	2.42	100%	2.4174	20	40	1.2V	1.93392	604	100	1.200826	1.93392	16.2	100
90W	AC+Battery	High	4.74	100%	4.8348	10	40	1.2V	1.93392	604	100	1.205686	1.93392	604	100
120W	AC+Battery	High	6.31	100%	6.4362	10	40	1.2V	2.57848	113	100	1.20676	2.57848	113	100
135W	AC+Battery	High	7.1	100%	7.242	10	40	1.2V	2.8968	180	100	1.207	2.8968	180	100

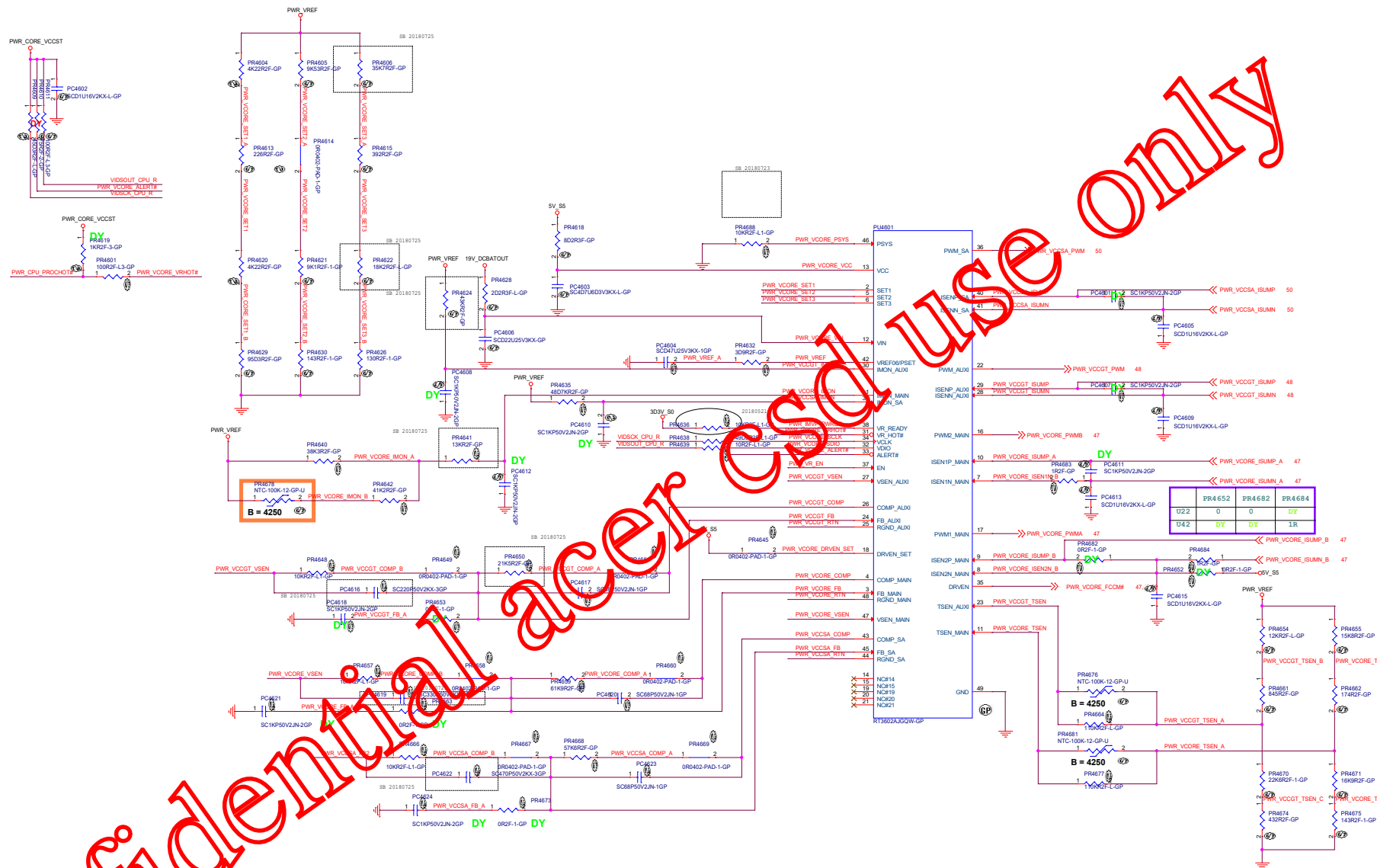
Wistron Corporation
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei 305, Taiwan, R.O.C.

044_Power (Charger_BQ24780S)

Doc Number: WLPiKaChu WL-1M

Rev: 1.00

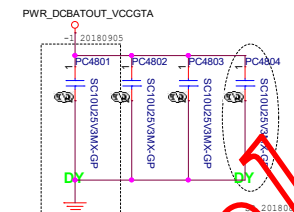
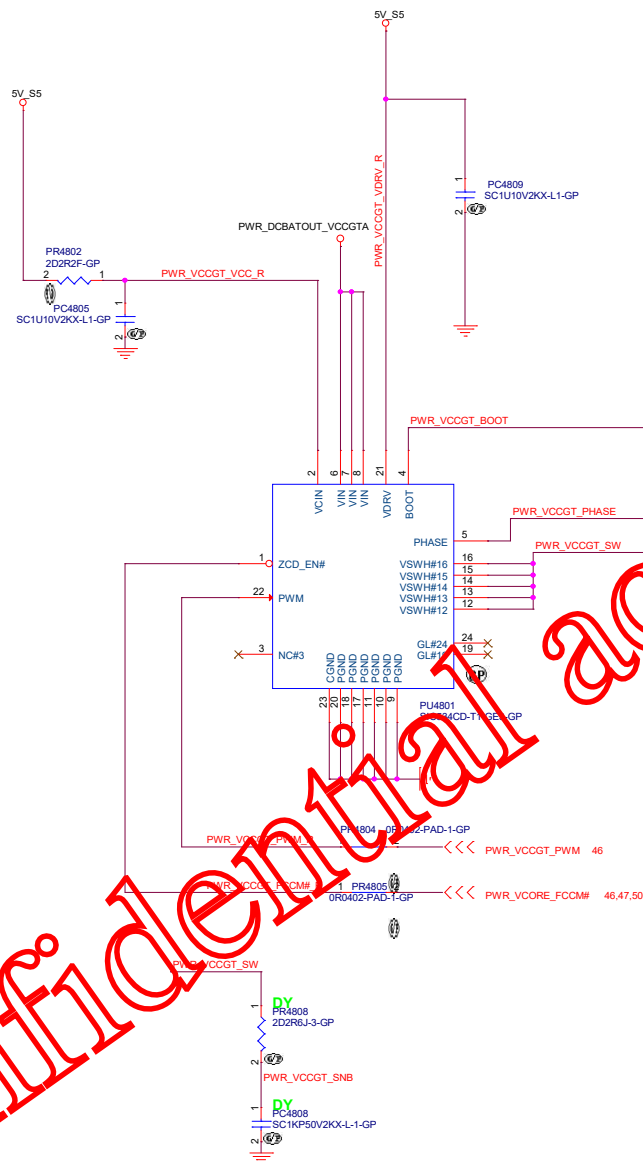
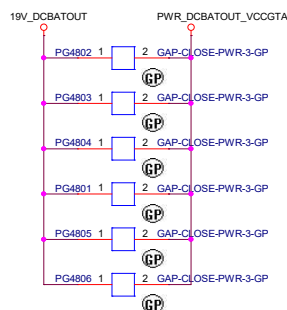
Main Func = CPU CORE



Main Func = CPU CORE

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA
HCB3225KF-151T50-GP
068.00005.0201
Vgt Vin Bead

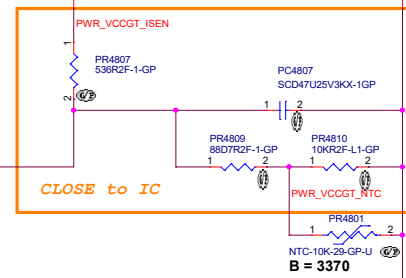
Co-Layer
Open-Gap



WHL_U42
Icc(max)=31A
TDC=18A
22uF/0603 total 13pcs

Cyntec . 6.8mm x7.6mm x4.0mm
DCR: 0.66m Ohm +/-7%
Idc : 36A , Isat : 45A

PL4801
COIL-D1511-2-GP
68.R1510.20A



1V_VCCGT
PT4801
SE330U2VDM-4-GP
PANASONIC
ESR: 9 mOhm
1st = 79.33719.20C
2nd = 077.53371.0081

46 PWR_VCCGT_ISUMP <<
46 PWR_VCCGT_ISUMN <<
Check

<Core Design>

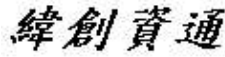
緯創資通 Wistron Corporation		
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.		
Title POWER (AOZ5049Q_VCCGT(3/3))		
Size Custom	Document Number Raichu_WL/Pikachu_WL	Rev -1M
Date: Tuesday, September 25, 2018	Sheet 48 of	108

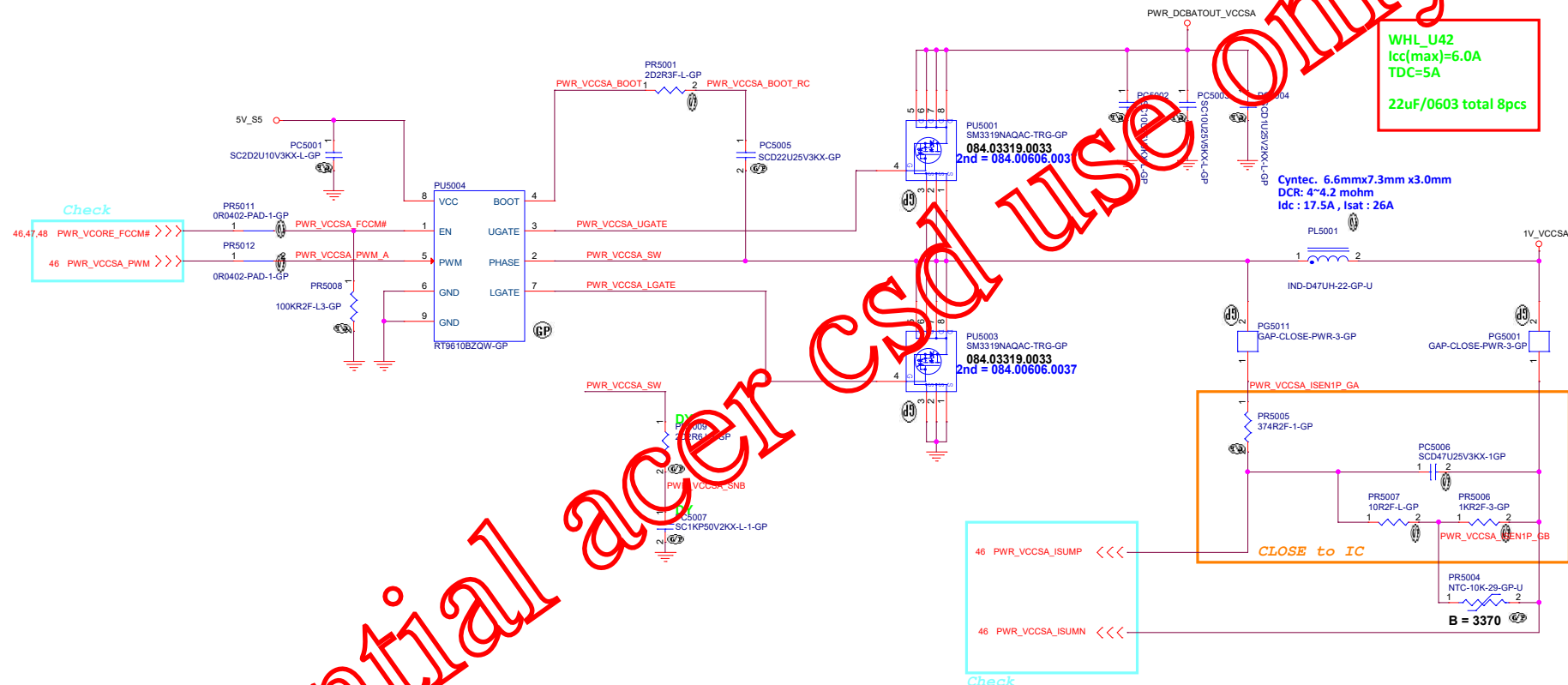
Low Noise MLCC

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Title Power (EE Reserved)			
Size A4	Document Number Raichu_WL/Pikachu_WL		Rev -1M
Date: Tuesday, September 25, 2018		Sheet 49 of	106



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Taipei Hsien 221, Taiwan, R.O.C.

CPU_ (Power CAP1)

Number	Rev
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Raichu WL/Pikachu WL -1

September 25, 2018 Sheet 50 of 106

OFFPAGE

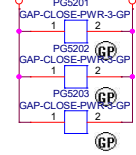
PH on EE Side

PWR_1D0V_PG

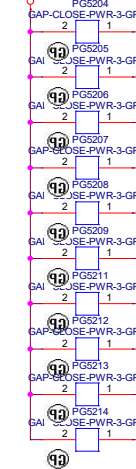
PWR_1D0V_EN

OFFPAGE_GAP

19V_DCBATOUT PWR_DCBATOUT_1D0V



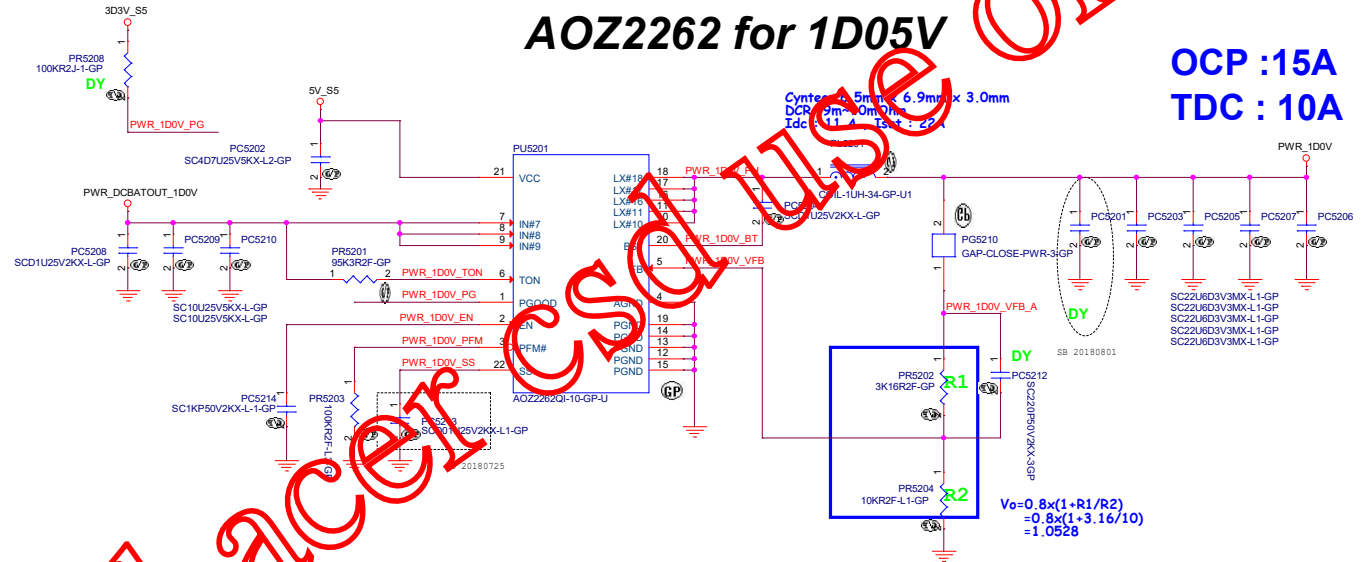
1D0V_S5 PWR_1D0V



SSID = PWR.Plane.Regulator_1p0v

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	074.02262.0043	074.02261.0A73	074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D05V

OCP :15A
TDC :10A

<Core Design>

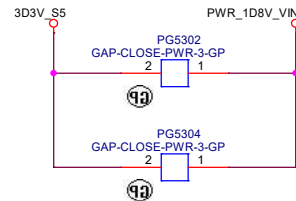
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Taippei Hsien 221, Taiwan, R.O.C.

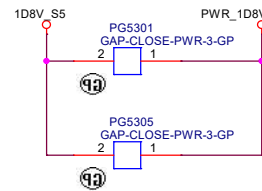
POWER (G5416_VDDQ/VTTP/VPP)			
Size	Document Number	Raichu_WL/Pikachu_WL	
Custom			Rev -1M
Date	Monday, September 25, 2018	Sheet 52	of 108

OFFPAGE

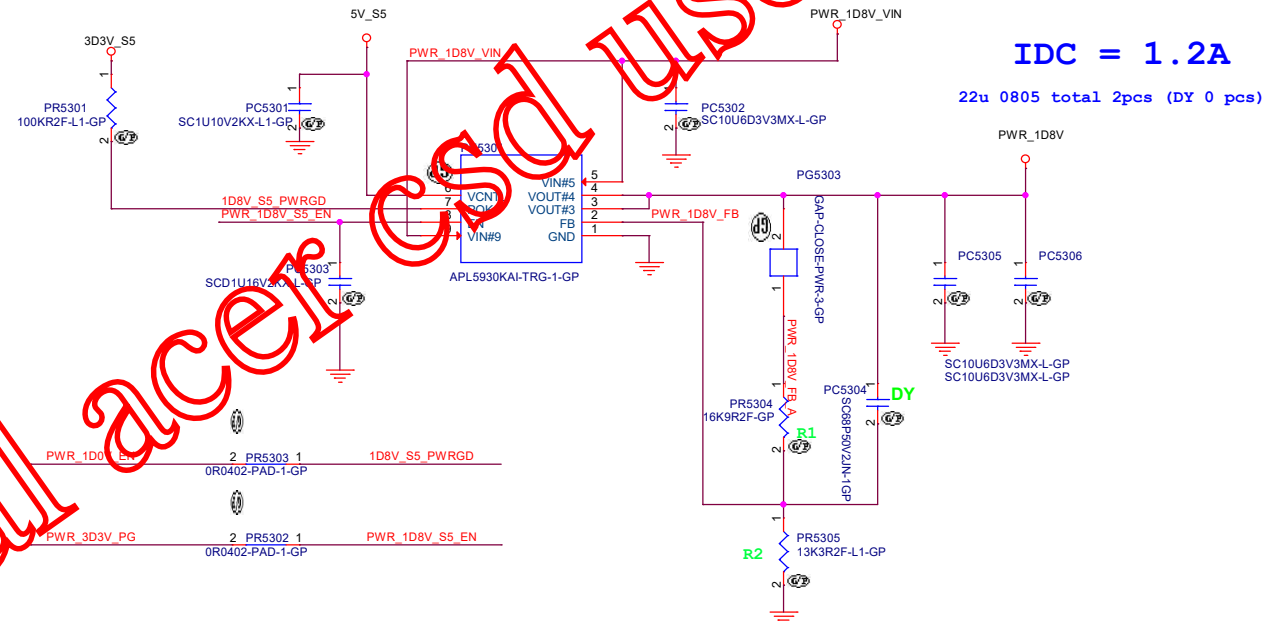
OFFPAGE_GAP



17.45 PWR_3D3V_PG >>>
52 PWR_1D0V_EN <<<



APL5930 for 1D8V



IDC = 1.2A

22u 0805 total 2pcs (DY 0 pcs)

$$\begin{aligned} V_{out} &= 0.8V \cdot (R1 + R2) / R2 \\ &= 0.8 \cdot (16.9 + 13.3) / 13.3 \\ &= 1.8165 \end{aligned}$$

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			POWER (APL5930_1D8V)	
Size	Document Number	Raichu_WL/Pikachu_WL		Rev
A3				-1M
Date:	Tuesday, September 25, 2018	Sheet	53	of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power (RSVD)

Size
A4

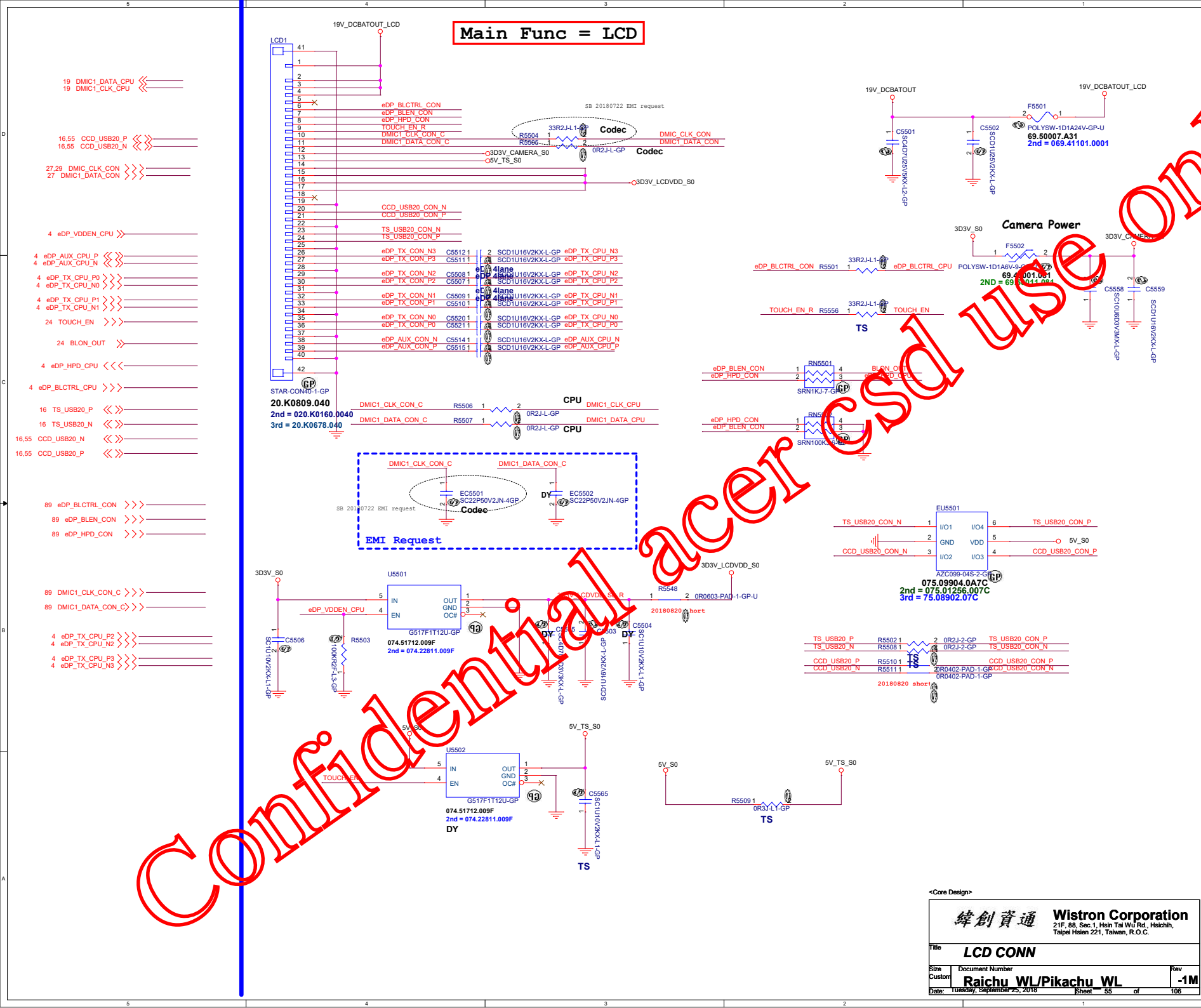
Document Number

Raichu_WL/Pikachu_WL

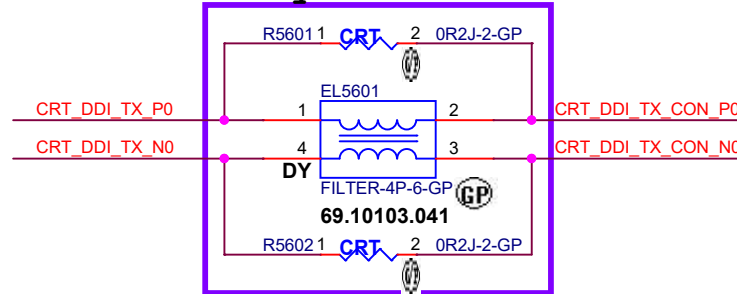
Rev
-1M

Date: Tuesday, September 25, 2018

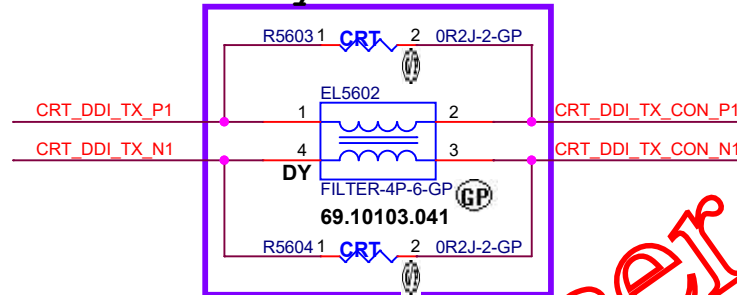
Sheet 54 of 106



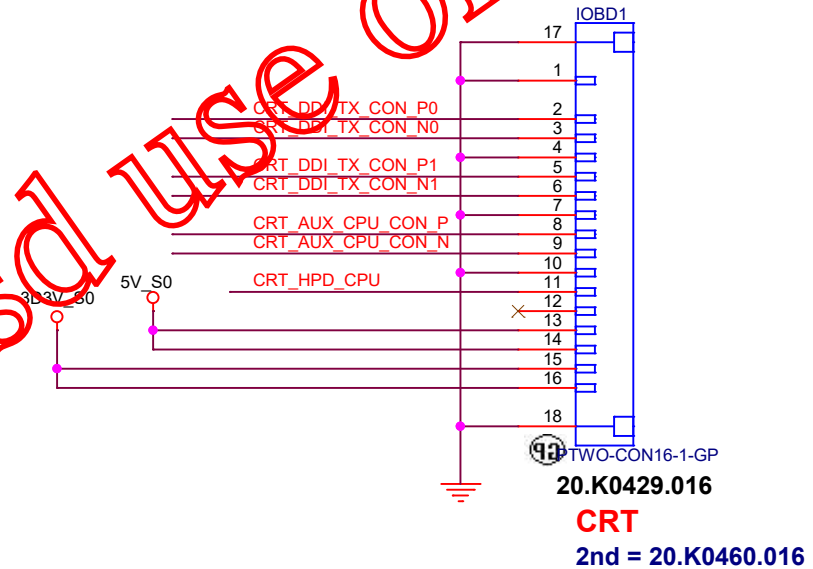
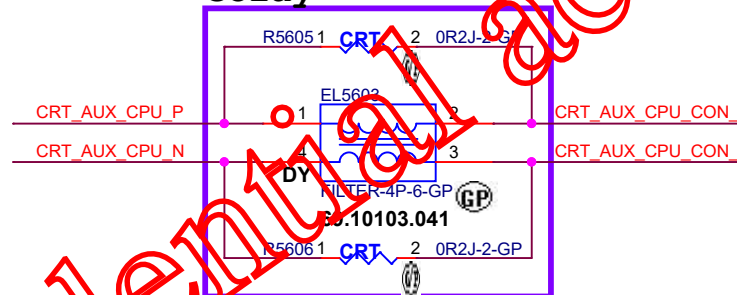
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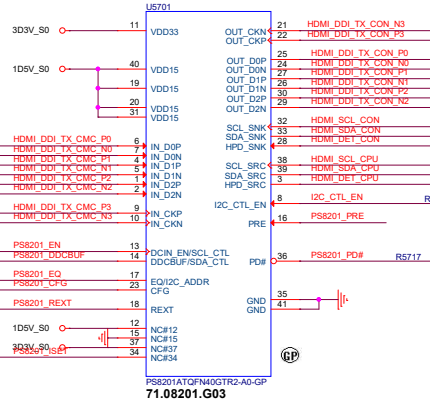
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HDMI 1.4 & CONNECTOR

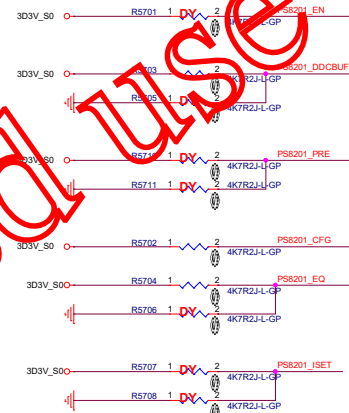
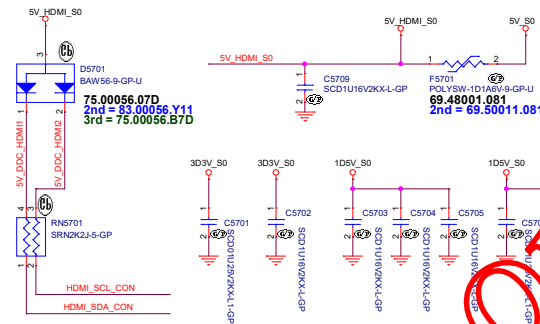
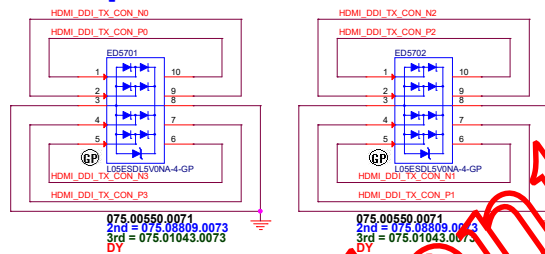
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4 HDMI_DDI_TX_N2
4 HDMI_DDI_TX_P3
4 HDMI_DDI_TX_N3
4 HDMI_SCL_CPU
4 HDMI_SDA_CPU
4 HDMI_DET_CPU

89 HDMI_DDI_TX_CON_P0
89 HDMI_DDI_TX_CON_N0
89 HDMI_DDI_TX_CON_P1
89 HDMI_DDI_TX_CON_N1
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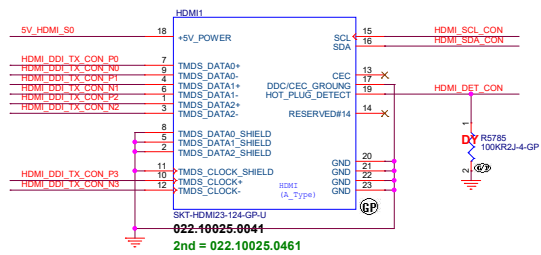
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HDMI_DDI_TX_P1 C5710 1 2 SCD1U16V2KX-L-GP
HDMI_DDI_TX_N1 C5712 1 2 SCD1U16V2KX-L-GP
HDMI_DDI_TX_P2 C5714 1 2 SCD1U16V2KX-L-GP
HDMI_DDI_TX_N2 C5713 1 2 SCD1U16V2KX-L-GP
HDMI_DDI_TX_P3 C5716 1 2 SCD1U16V2KX-L-GP
HDMI_DDI_TX_N3 C5715 1 2 SCD1U16V2KX-L-GP



EMI Request:



HDMI CONN



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number

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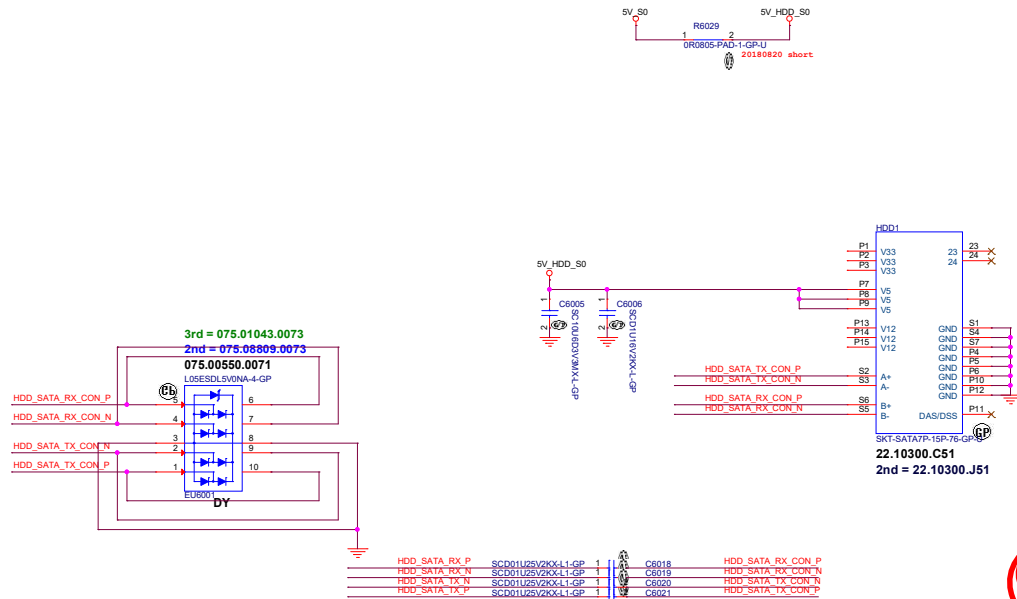
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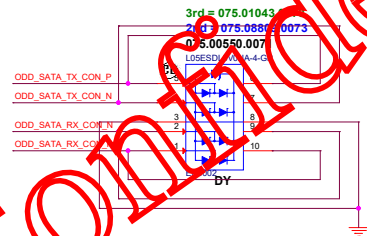
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SSID = SATA SATA HDD Connector



ODD Connector

AC coupling caps near connector<100 pF



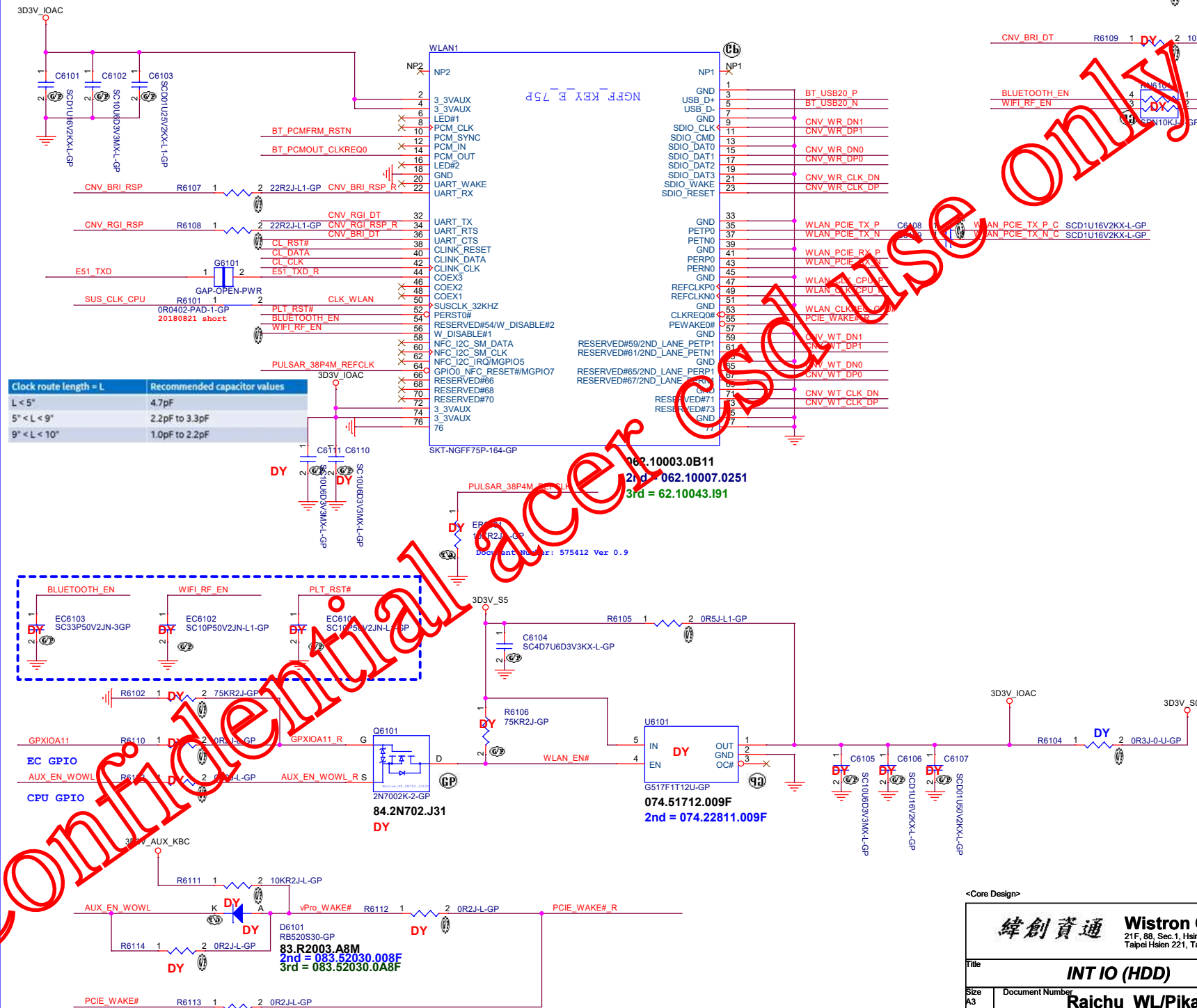
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SSID = Wireless Mini Card Connector(802.11a/b/g/n)

24.68 E51_TXD
16.89 BT_USB20_N
16.89 BT_USB20_P
17.24,31.63,68.79,89.91 PLT_RST#
24.89 BLUETOOTH_EN
24.89 WIFI_RF_EN
16 WLAN_PCIE_TX_P_C
16 WLAN_PCIE_TX_N_C
16.89 WLAN_PCIE_RX_P
16.89 WLAN_PCIE_RX_N
18.89 WLAN_CLK_CPU_P
18.89 WLAN_CLK_CPU_N
18.89 WLAN_CLKREQ_CPU#
17.31,63.89 PCIE_WAKE#
21 CNV_WR_DN0
21 CNV_WR_DP0
21 CNV_WR_DN1
21 CNV_WR_DP1
21 CNV_WT_DN0
21 CNV_WT_DP0
21 CNV_WT_DN1
21 CNV_WT_DP1
21 CNV_WR_CLK_DN
21 CNV_WR_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_CLK_DP
19 BT_PCMFRM_RSTN
20 CNV_BRI_RSP
20 CNV_RGI_DT
20 CNV_RGI_RSP
20 CNV_BRI_DT
18 PULSAR_38P4M_REFCLK
18 SUS_CLK_CPU
17 AUX_EN_WOWL
24 GPXIOA11
89 WLAN_PCIE_TX_P
89 WLAN_PCIE_TX_N
18 CL_RST#
18 CL_DATA
18 CL_CLK



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SSID = mSATA

Mini Card Connector(mSATA)

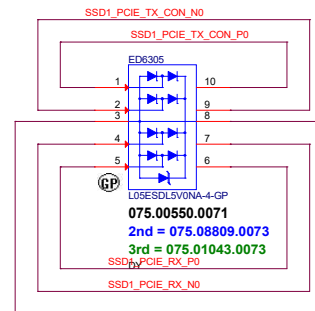
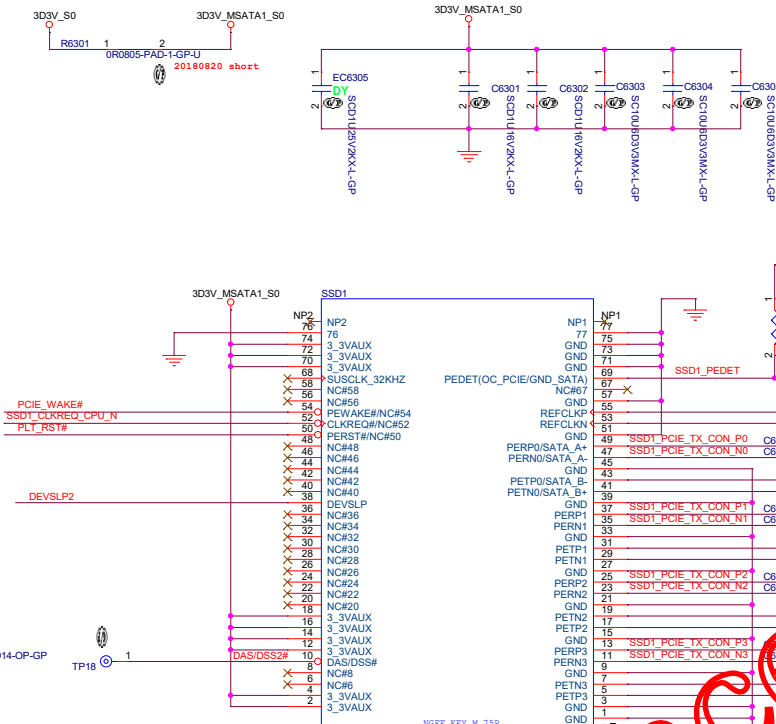
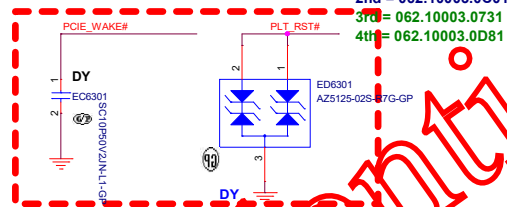


Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe® Controller #1				PCIe® Controller #2				PCIe® Controller #3			
Flex I/O Lane #	PCIe Lane #	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	1x4	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x1+1x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-U	1x4	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x1+1x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-Y	1x4	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	2x1+1x2	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12



Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Processor	100 nF	220 nF	10 nF	100 nF	220 nF
Processor	None	None	10 nF ²	None	None ³

Note:

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe lane that needs to support either **PCIe® Gen2 devices** or **PCIe® Gen3 devices**, follow the PCIe Gen 3 / SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes			Module Type and Main Host Interface ¹		Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	NC	GND	GND	SSD - PCIe	N/A

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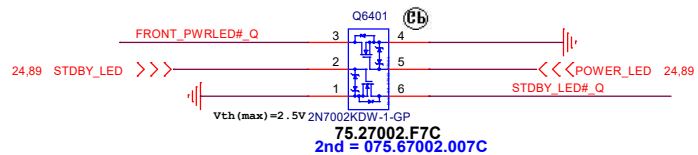
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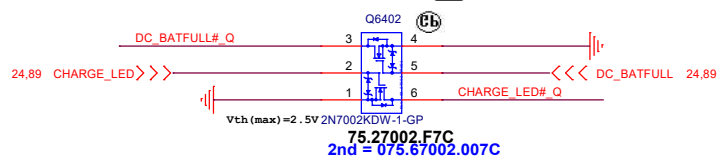
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Power button LED

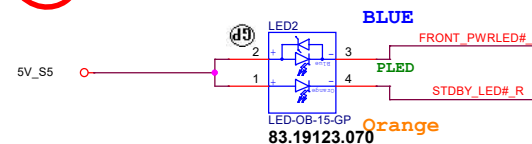
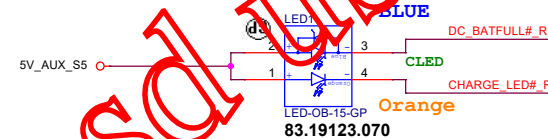
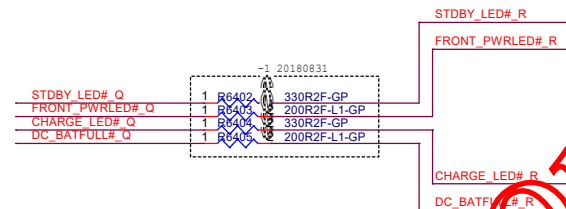


Power STDBY_LED

Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



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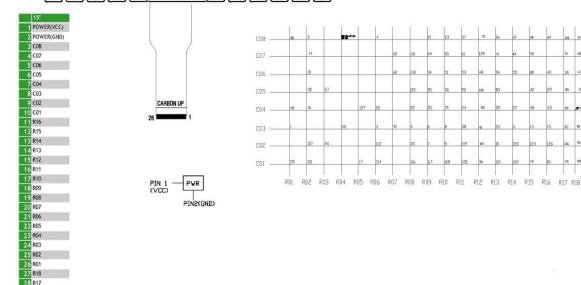
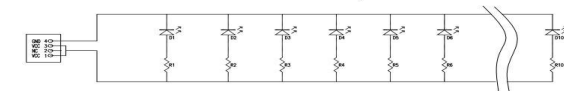
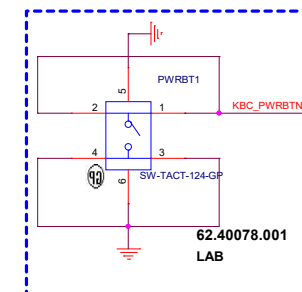
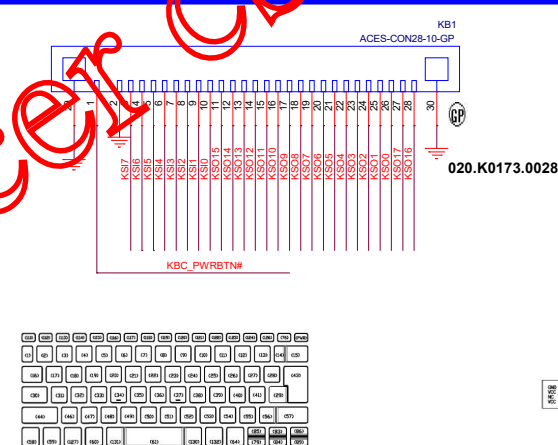
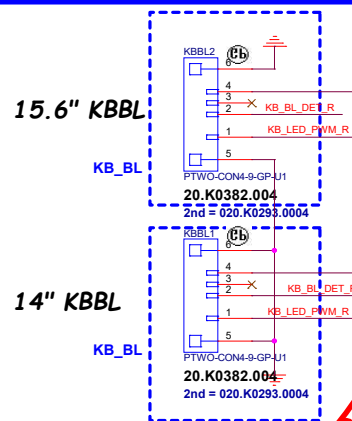
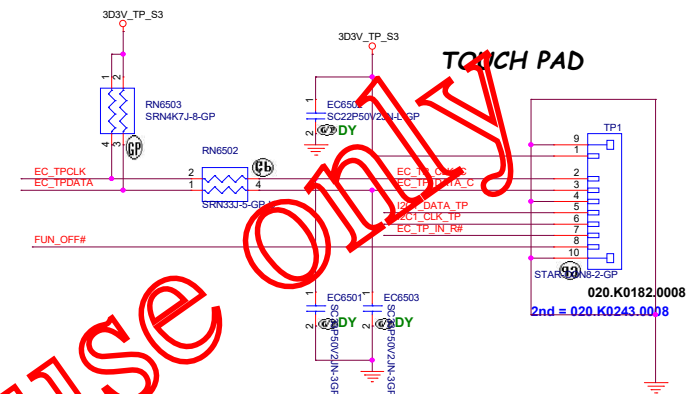
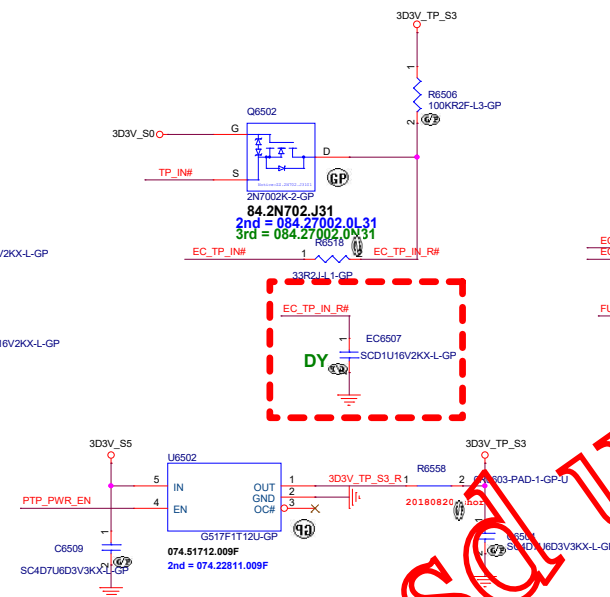
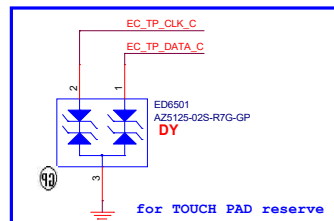
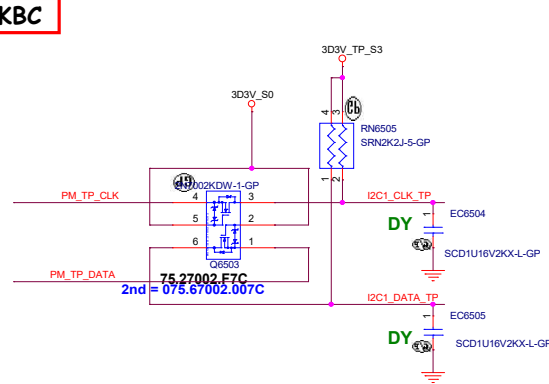
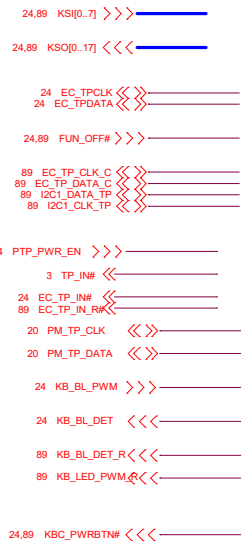
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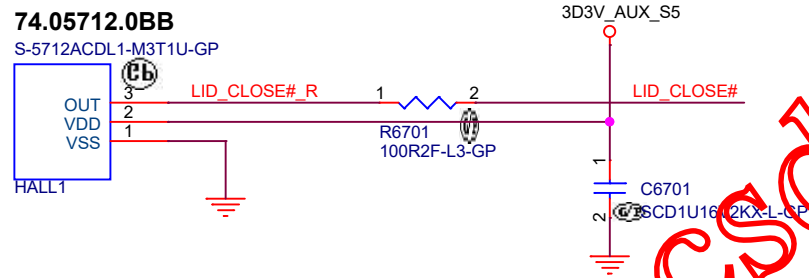
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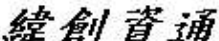
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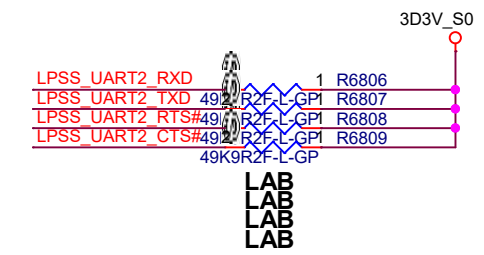
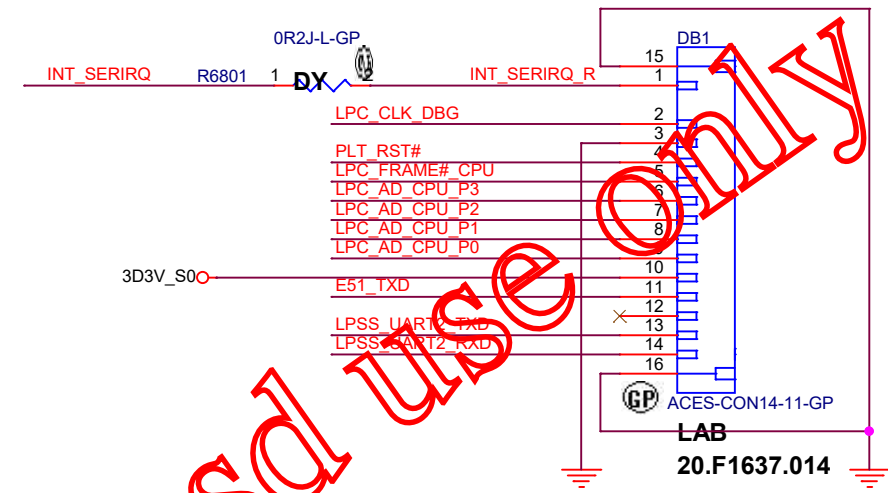
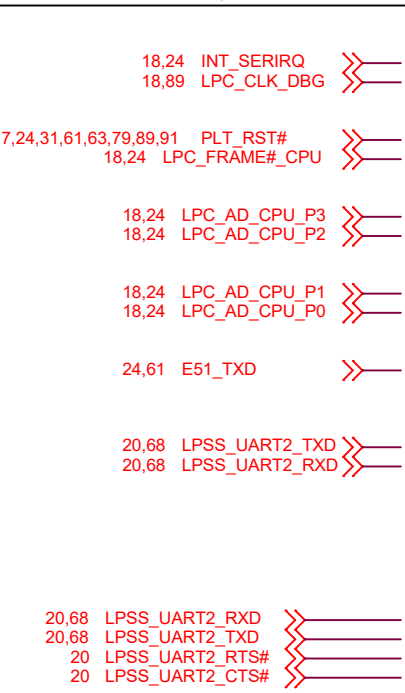
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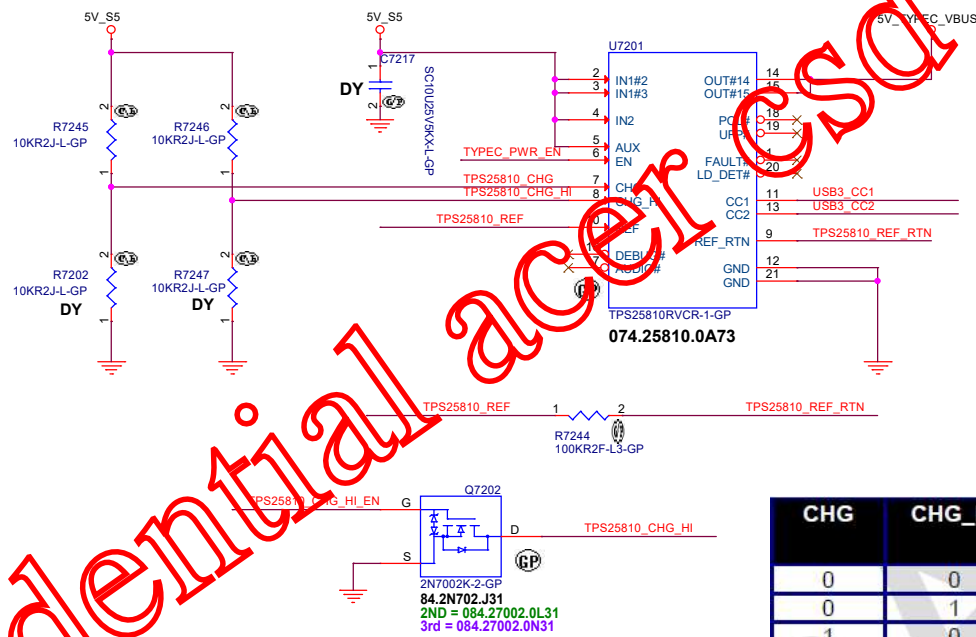
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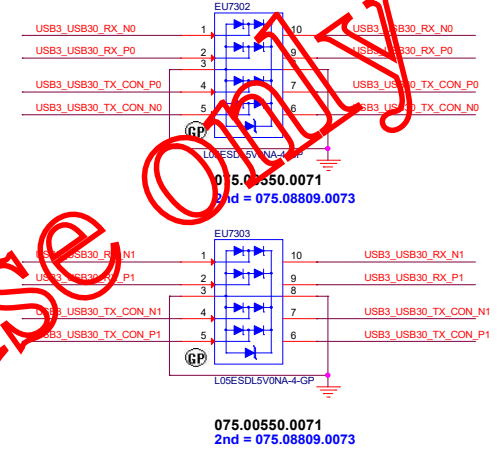
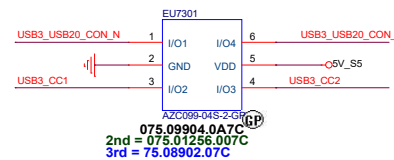
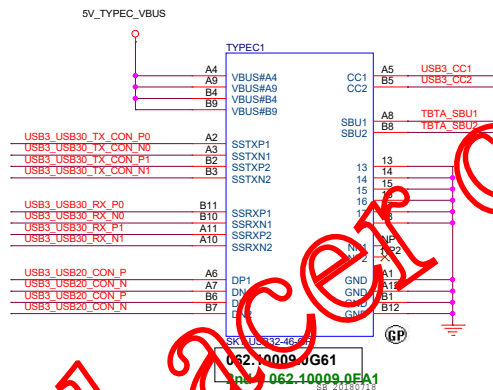
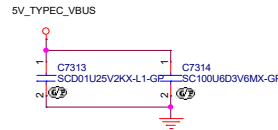
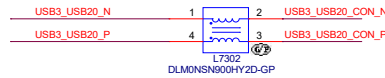
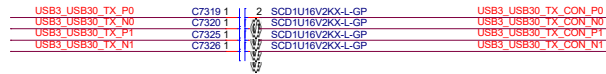
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USB HOST



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Title

EXT IO (RSVD)

Size
A4

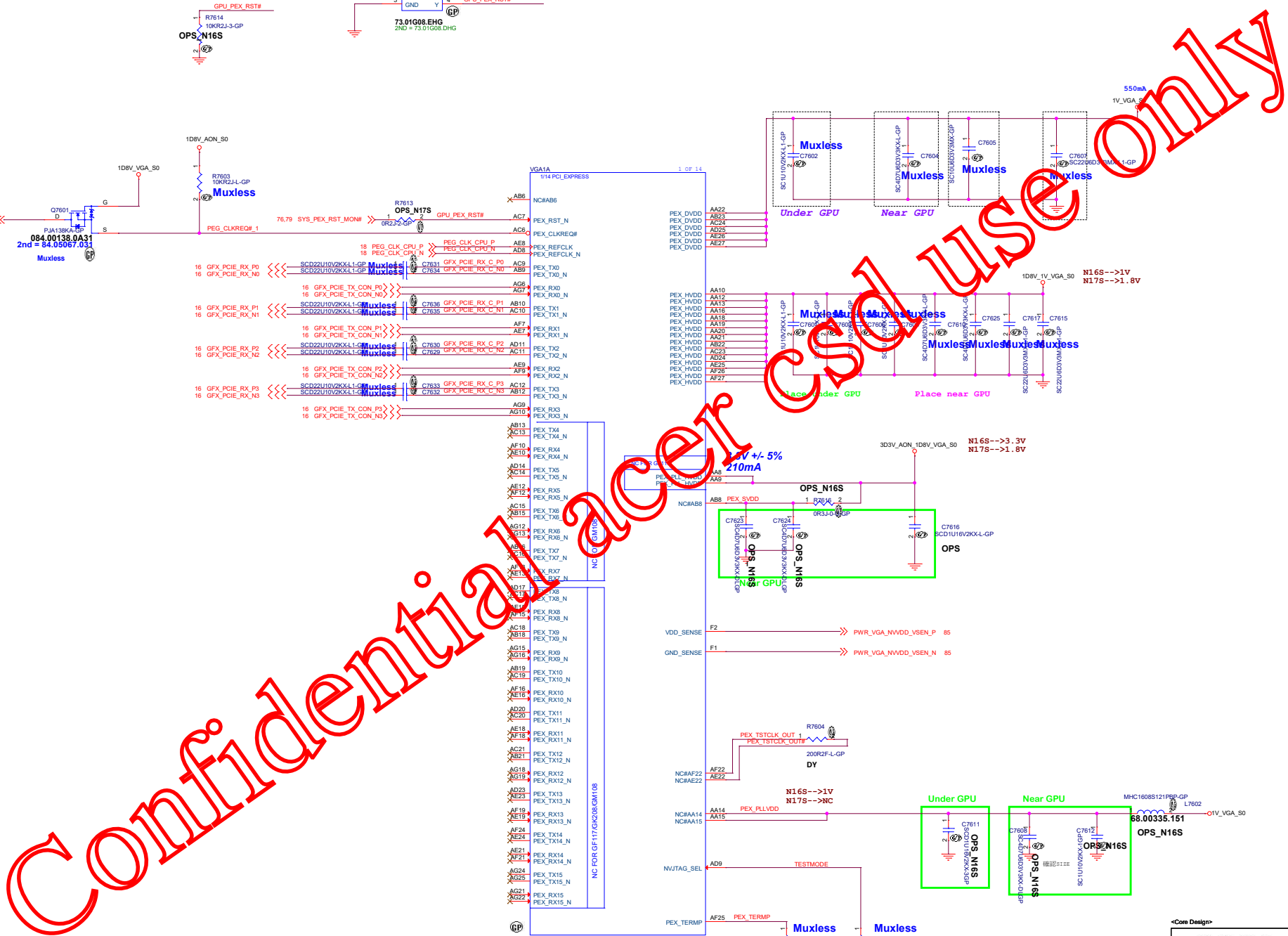
Document Number

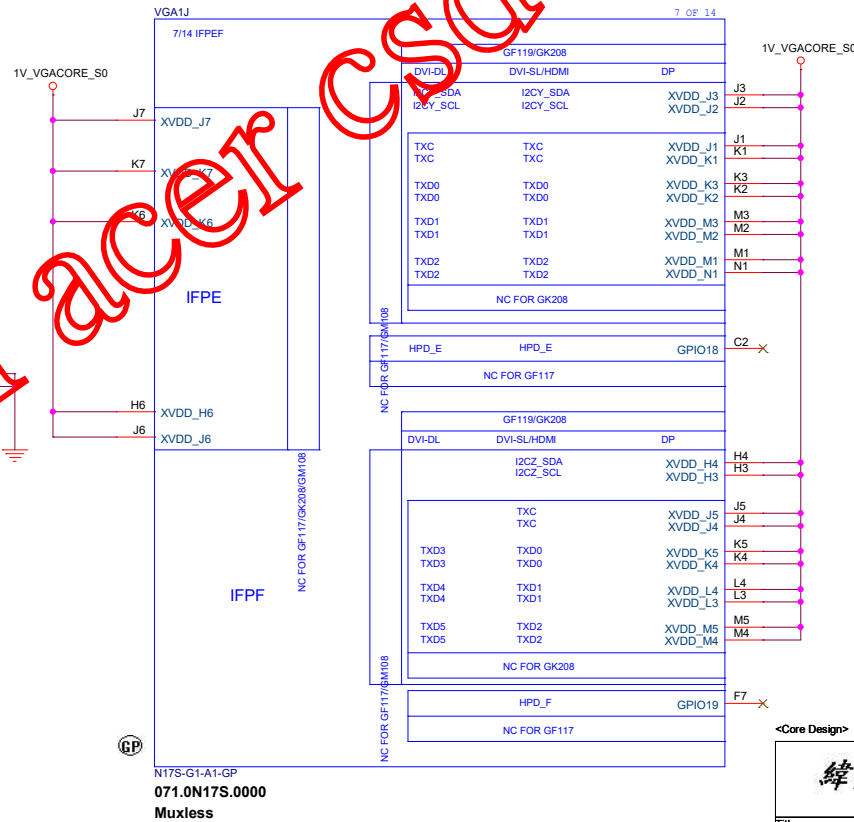
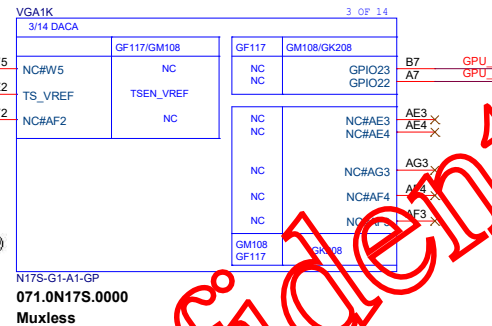
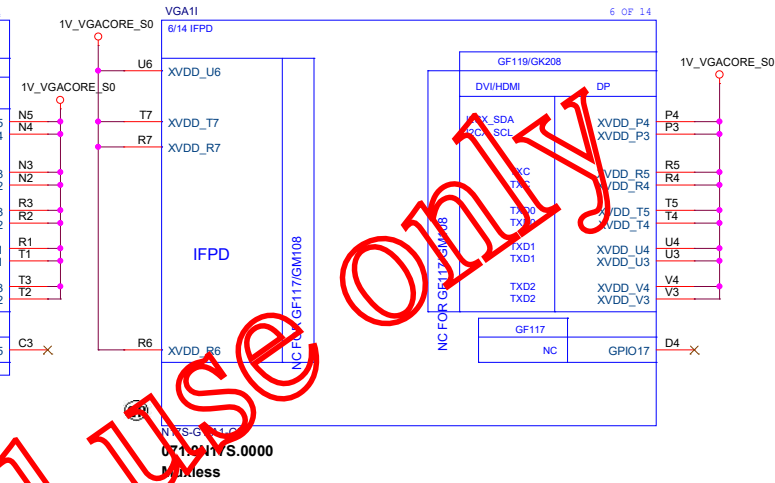
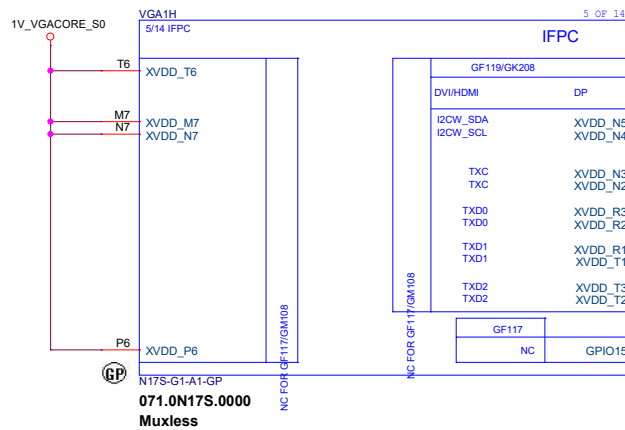
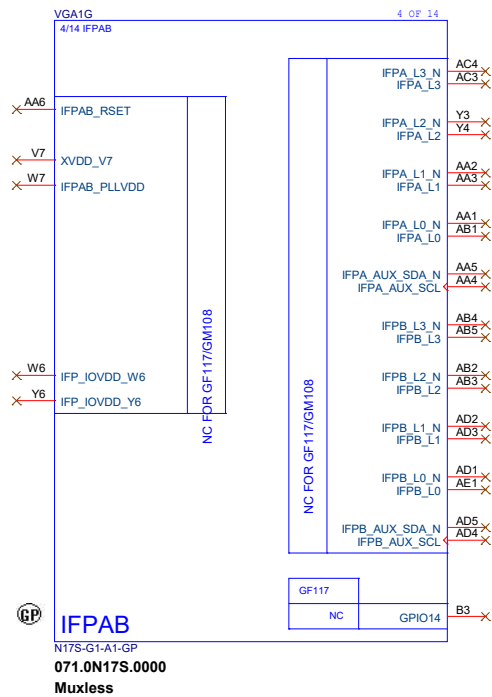
Raichu_WL/Pikachu_WL

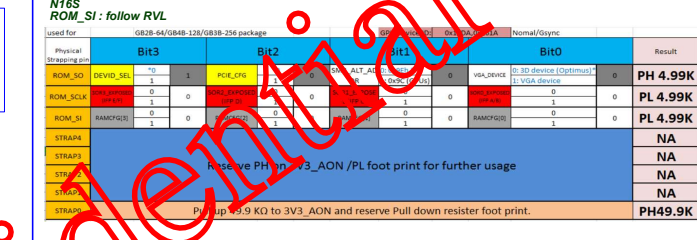
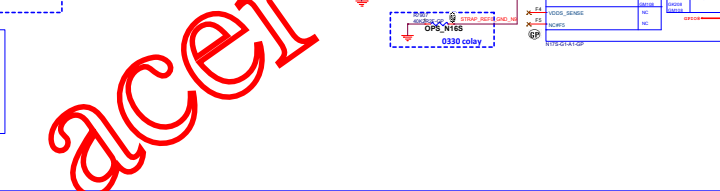
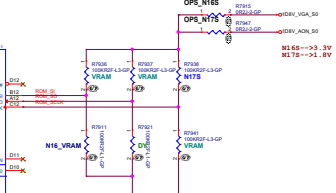
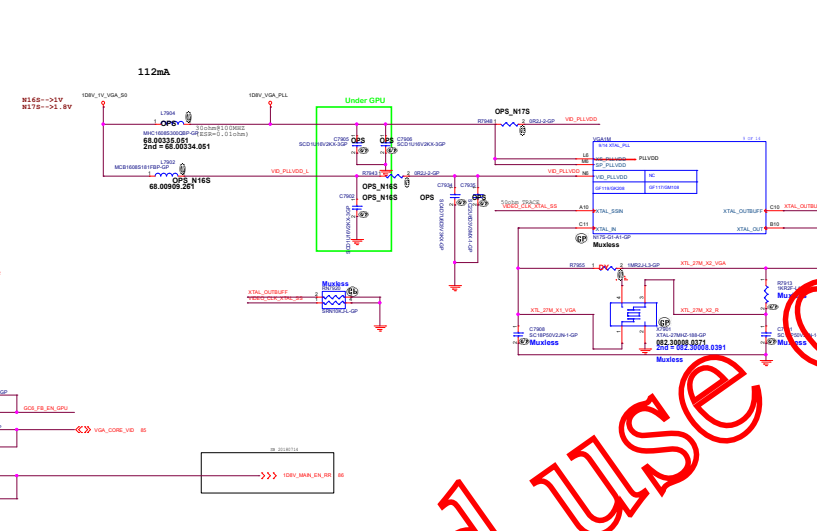
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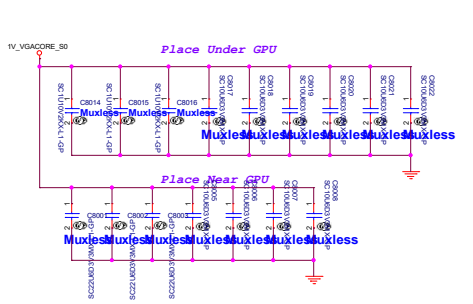




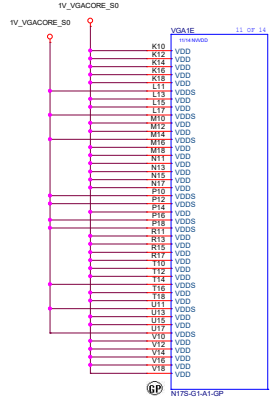


Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Data Code Minimum	Status
			Samsung	K4C80325FB-HC25	B-die	0x0	2500	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC8H24MR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24MR-ROC	M-die	0x5	3000	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC8H24MR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver ¹
			Micron	MT51J256M32HF-60.A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70.A	A-die	0x1	3000	N/A	Substitution allowed with waiver ¹
			Micron	MT51J256M32HF-80.A	A-die	0x1	3000	N/A	Substitution allowed with waiver ¹
			Micron	MT51J256M32HF-70.B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80.B	B-die	0x8	3000	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC8H24JR-ROC	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24JR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver ²

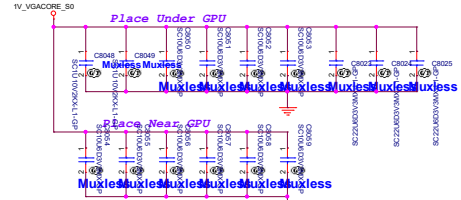
Memory Density	Allowed Memory Configuration	FBDVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	256Axx32 512Axx16	1.35V	Samsung	K4GB0325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4GB0325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Substitution allowed with valver ¹
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-B0:A	A-die	0x1	8 Gbps	N/A	Full	Substitution allowed with valver ¹
			Hynix	H5GCBH24AJR-R0C	A-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GCBH24AJR-R0C	A-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with valver ¹
			Micron	MT51J256M32HF-70:B	B-die	0x2	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-B0:B	B-die	0x2	8 Gbps	N/A	Full	Substitution allowed with valver ¹
			Hynix	H5GCBH24AJR-R0C	A-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GCBH24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with valver ¹



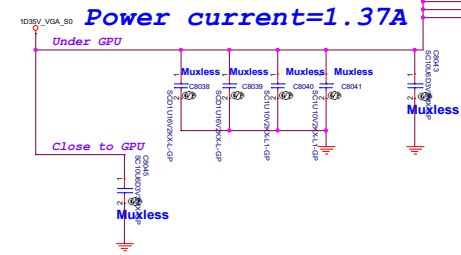
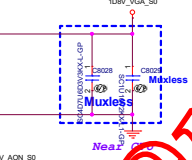
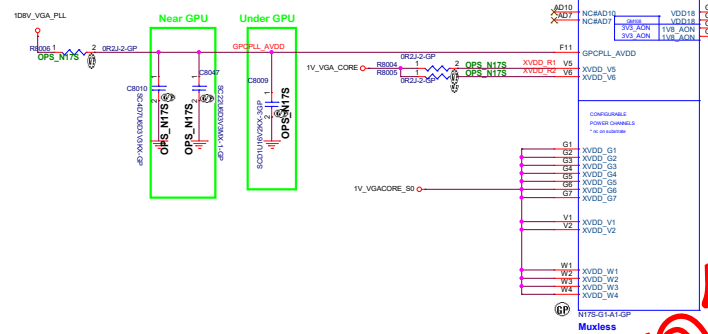
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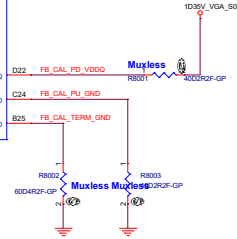
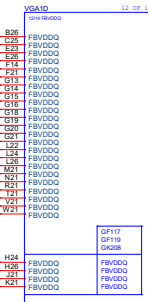
Power current=26A



Power current=60mA



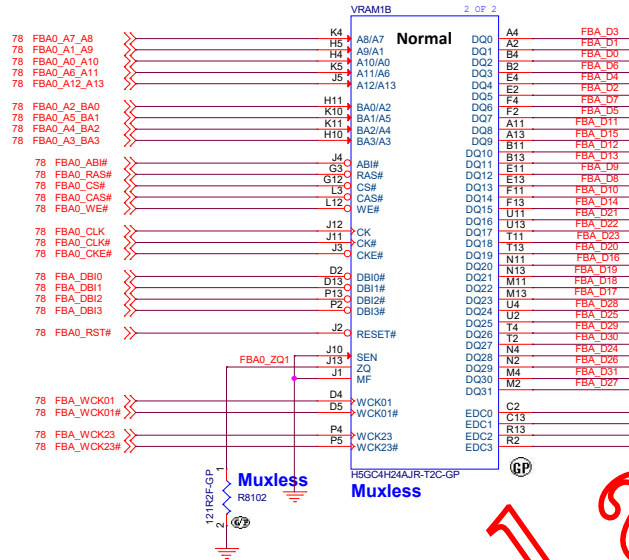
Power current=1.37A



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78 FBA_D[63:0] <<>

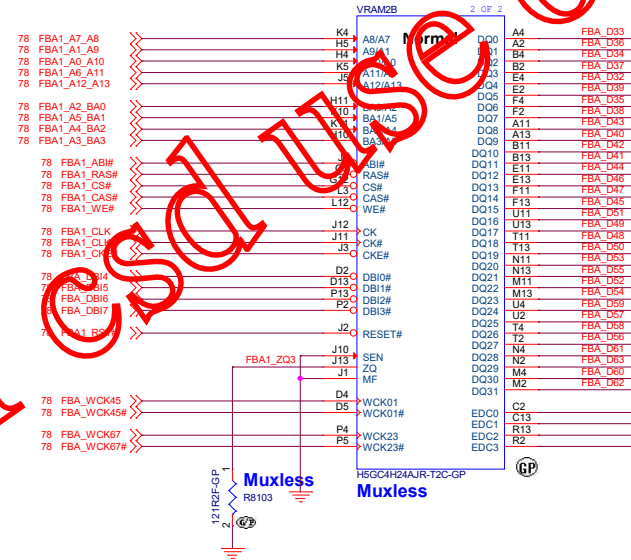


Byte 0
0~7

Byte 1
8~15

Byte 2
16~23

Byte 3
24~31



Byte 4
32~39

Byte 5
40~47

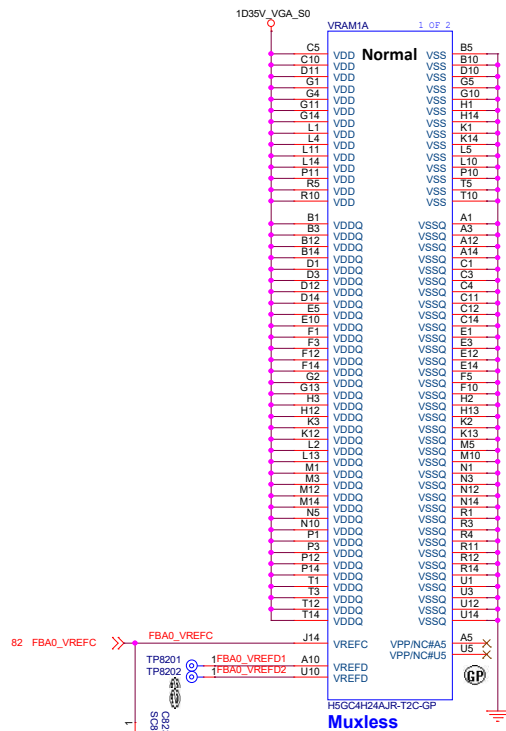
Byte 6
48~55

Byte 7
56~63

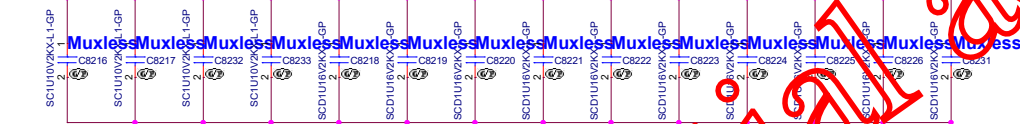
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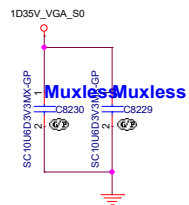
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Size	Document Number	Rev	
Custom			Raichu_WL/Pikachu_WL-1M
Date:	Tuesday, September 25, 2018	Sheet	81 of 106



FOR VRAM2



CLOSE TO THE MEMORY



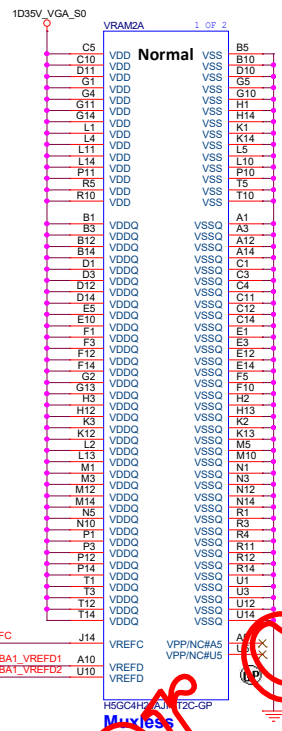
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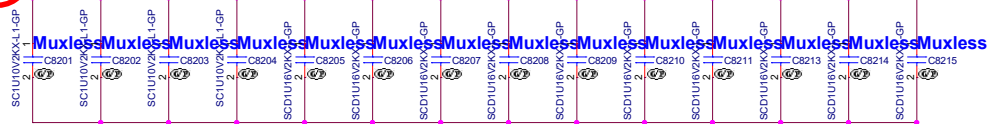
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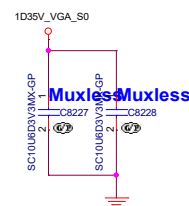
Muxless



FOR VRAM1



CLOSE TO THE MEMORY



NEAR VRAM1

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Title	VRAM POWER	
Size	Document Number	Rev
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Title

GPU (RSVD)

Size
A4

Document Number

Raichu_WL/Pikachu_WL

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Title

GPU (RSVD)

Size
A4

Document Number

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SSID = PWR.Plane.Regulator_ip0v

SSID = PWR.Plane.Regulator_ip35v

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Chock		68.1801A.20B	68.1801A.20B	68.1801A.20B
		ZDC : 1.10A	ZDC : 1.10A	ZDC : 1.0A
Output CAP		22uF/6.3V + 5pcs	22uF/6.3V + 4pcs	22uF/6.3V + 4pcs
		DV*1	DV*1	DV*1

AOZ2262 for 1D35V

TDC : 8.6A
Peak : 10.3A

Cytec: 6.5mm x 6.9mm x 3.0mm
DCR: 9m-10mOhm
Idc : 11 A, Isat : 22A

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2nd = 074.05335.0043

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2nd = 074.05335.0043

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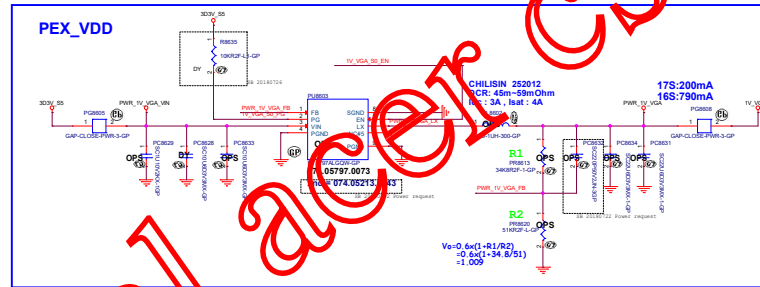
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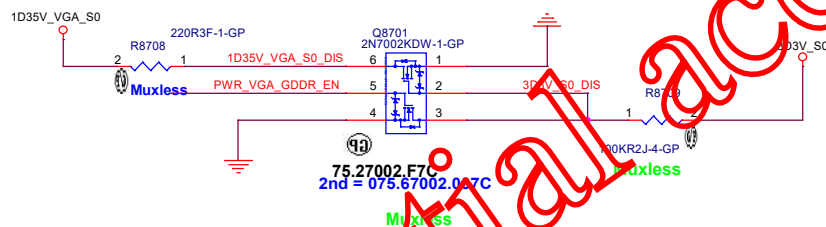
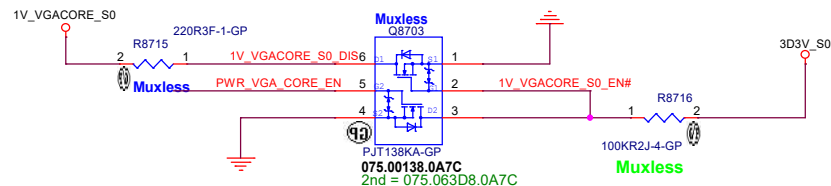
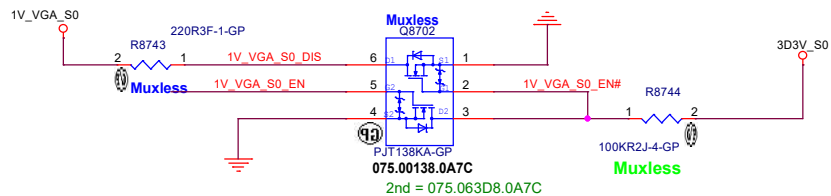
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FOR N17S
FOR N16S
FOR N17S
FOR N16S

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1.8V_AON_S0

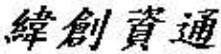


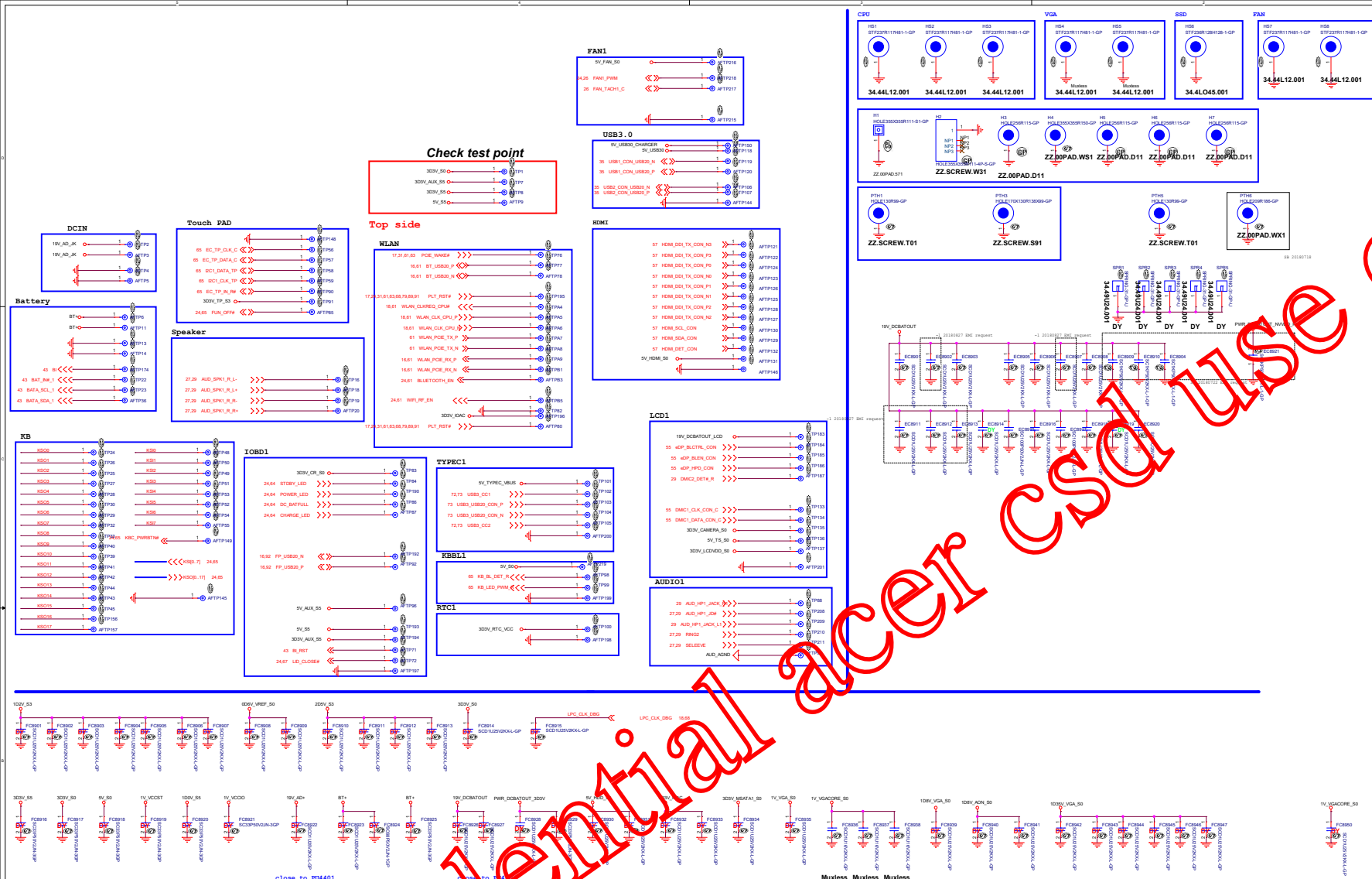
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Title		
Discharge		
Size	Document Number	Rev
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Title UNUSED PARTS (RSVD)			
Size A4	Document Number Raichu_WL/Pikachu_WL		Rev -1M
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Title

INT IO (RSVD)

Size
A4

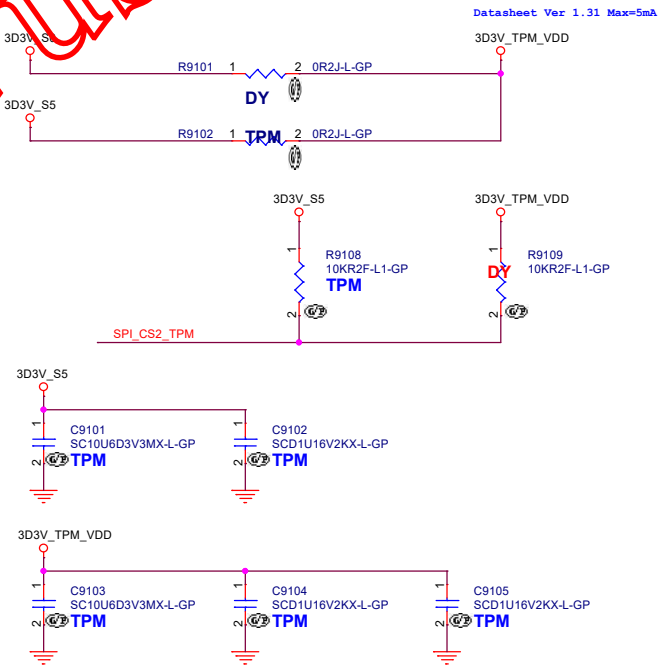
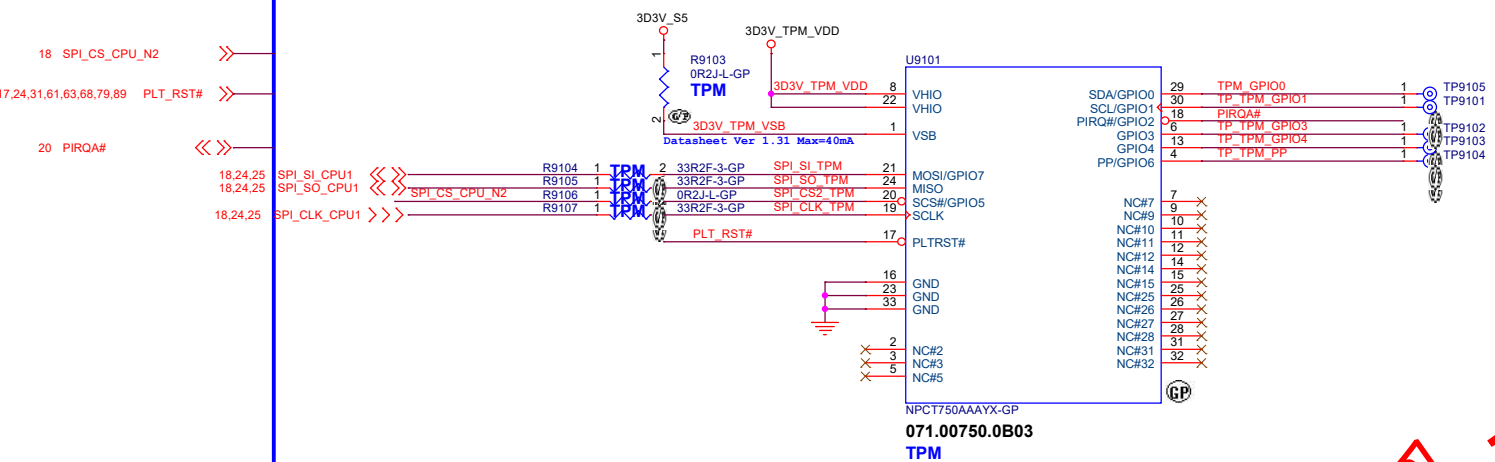
Document Number

Raichu_WL/Pikachu_WL

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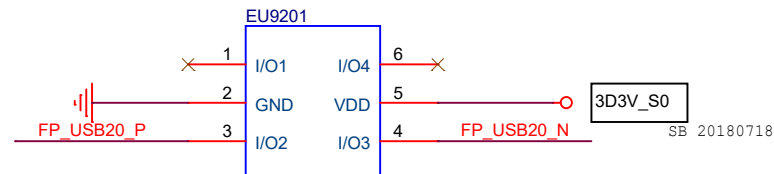
Signal	Resistor Type	Value	Notes
SPI0_CLK	Pull-down	20 kohm \pm 30%	
SPI0_MOSI	Pull-up	20 kohm \pm 30%	Note
SPI0_MISO	Pull-up	20 kohm \pm 30%	Note
SPI0_CS[2:0]#	Pull-down	20 kohm \pm 30%	
SPI0_IO[2:3]	Pull-up	20 kohm \pm 30%	Note

The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

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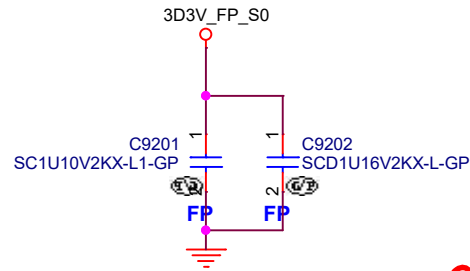
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Title INT IO (TPM)		
Size A3	Document Number Raichu_WL/Pikachu_WL	Rev -1M
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16,89 FP_USB20_P
16,89 FP_USB20_N



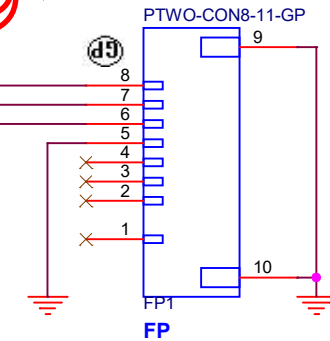
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3rd = 75.08902.07C

FP



3D3V_FP_S0

FP_USB20_P
FP_USB20_N



20.K0767.008
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3rd = 020.K0328.0008



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Commercial (RSVD)

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Size
A4

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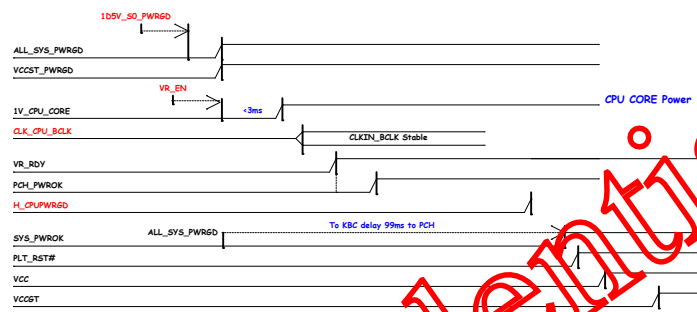
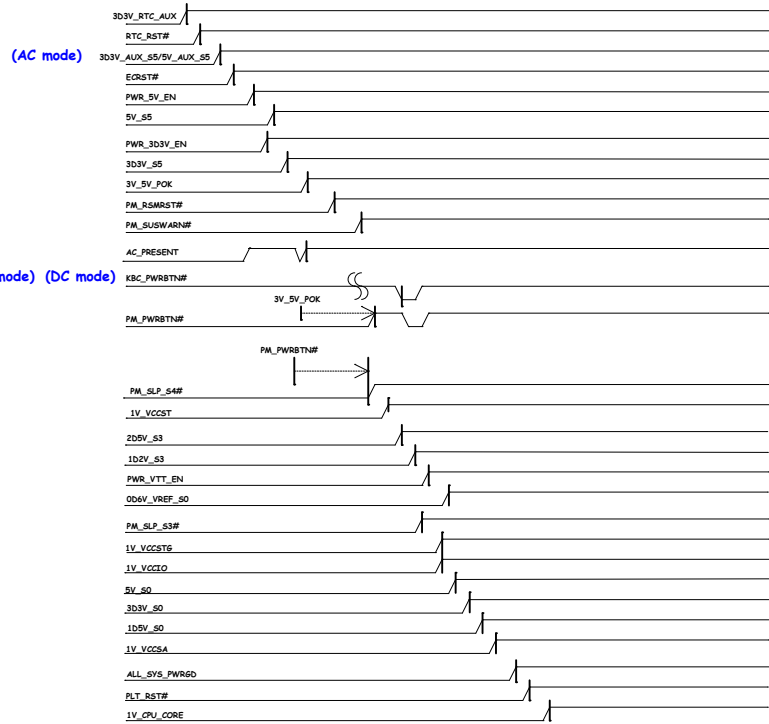
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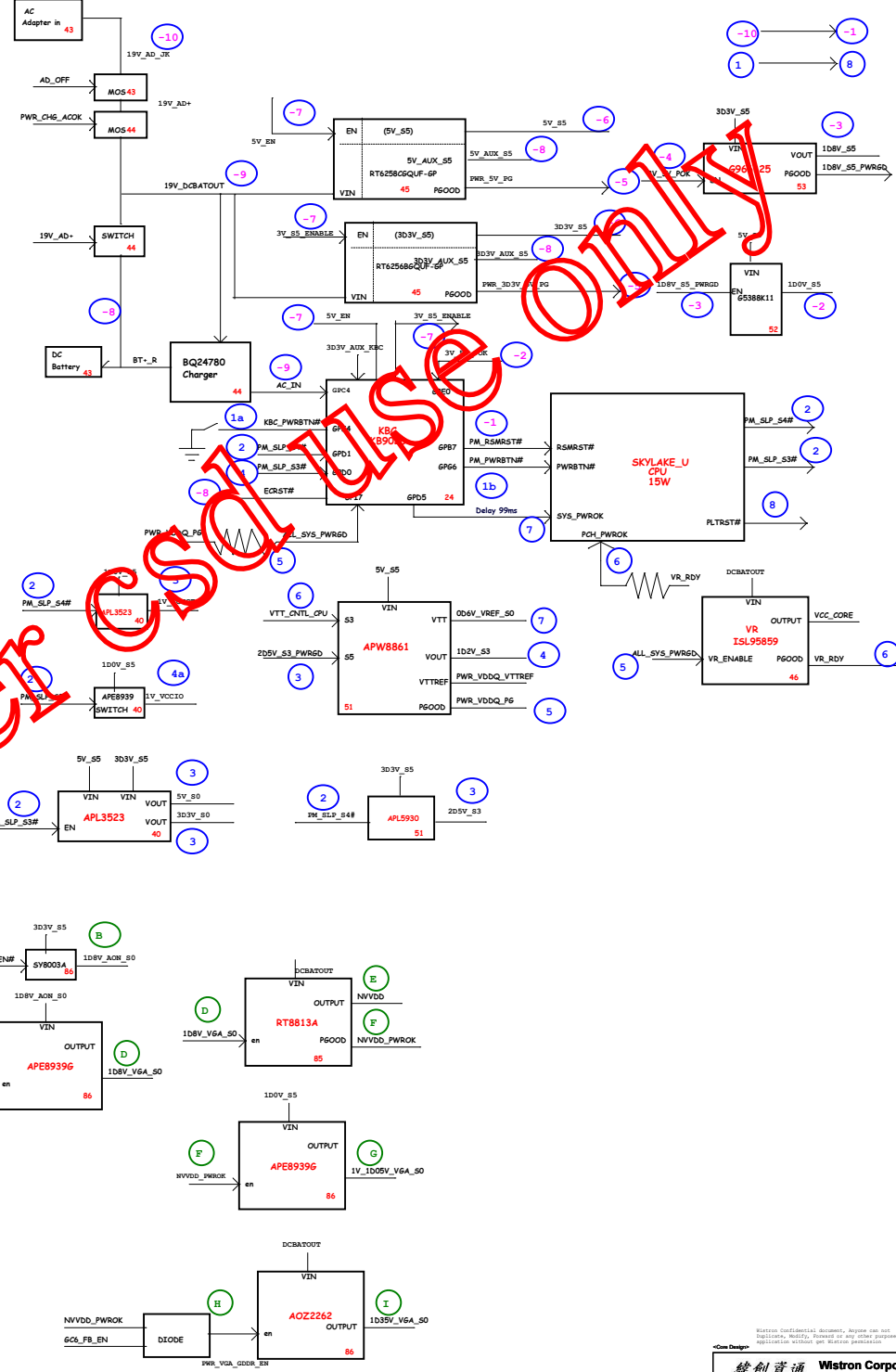
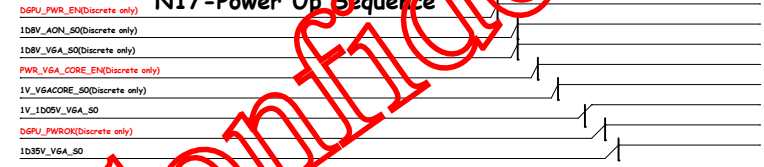
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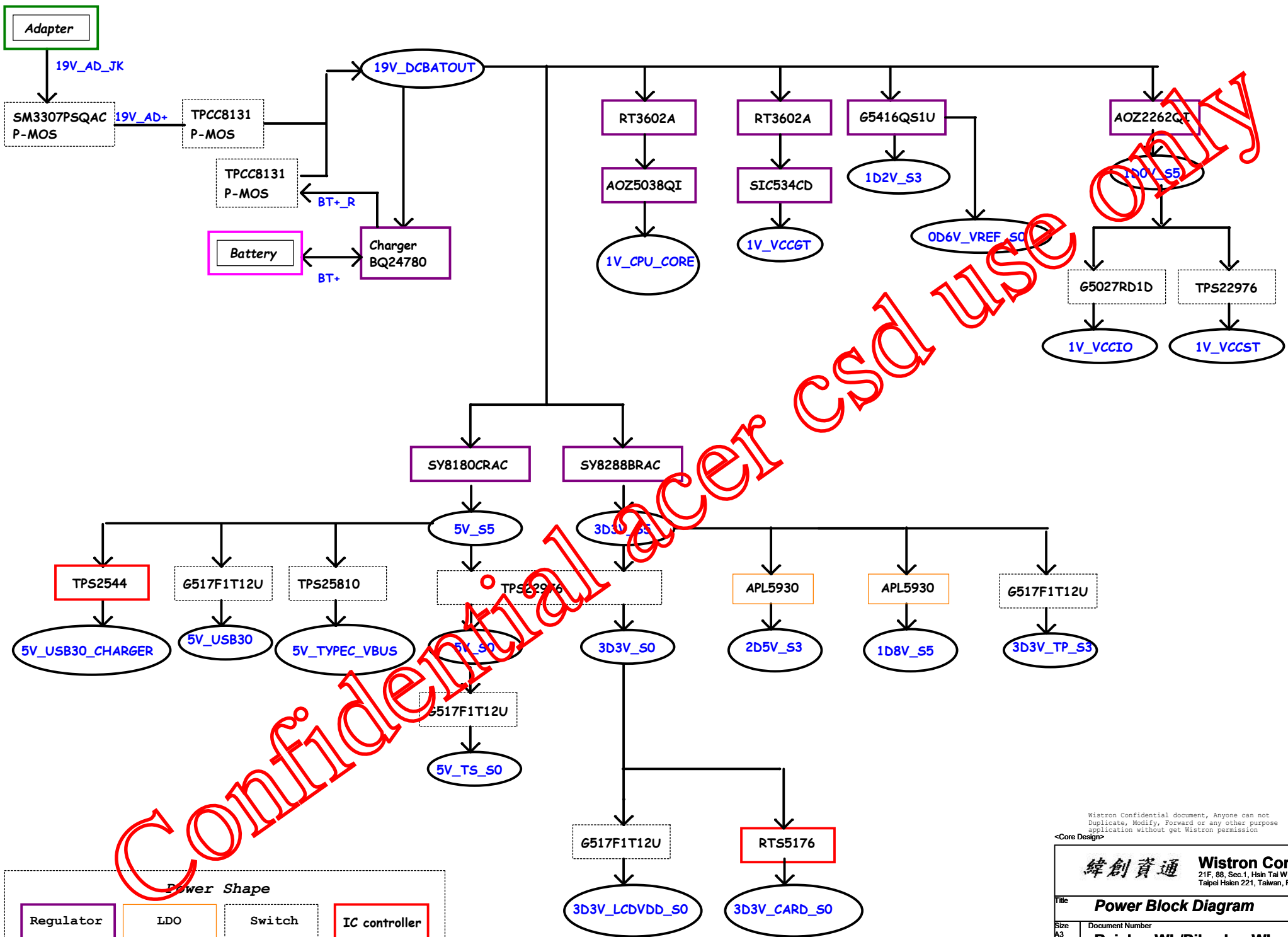
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Intel-Power Up Sequence

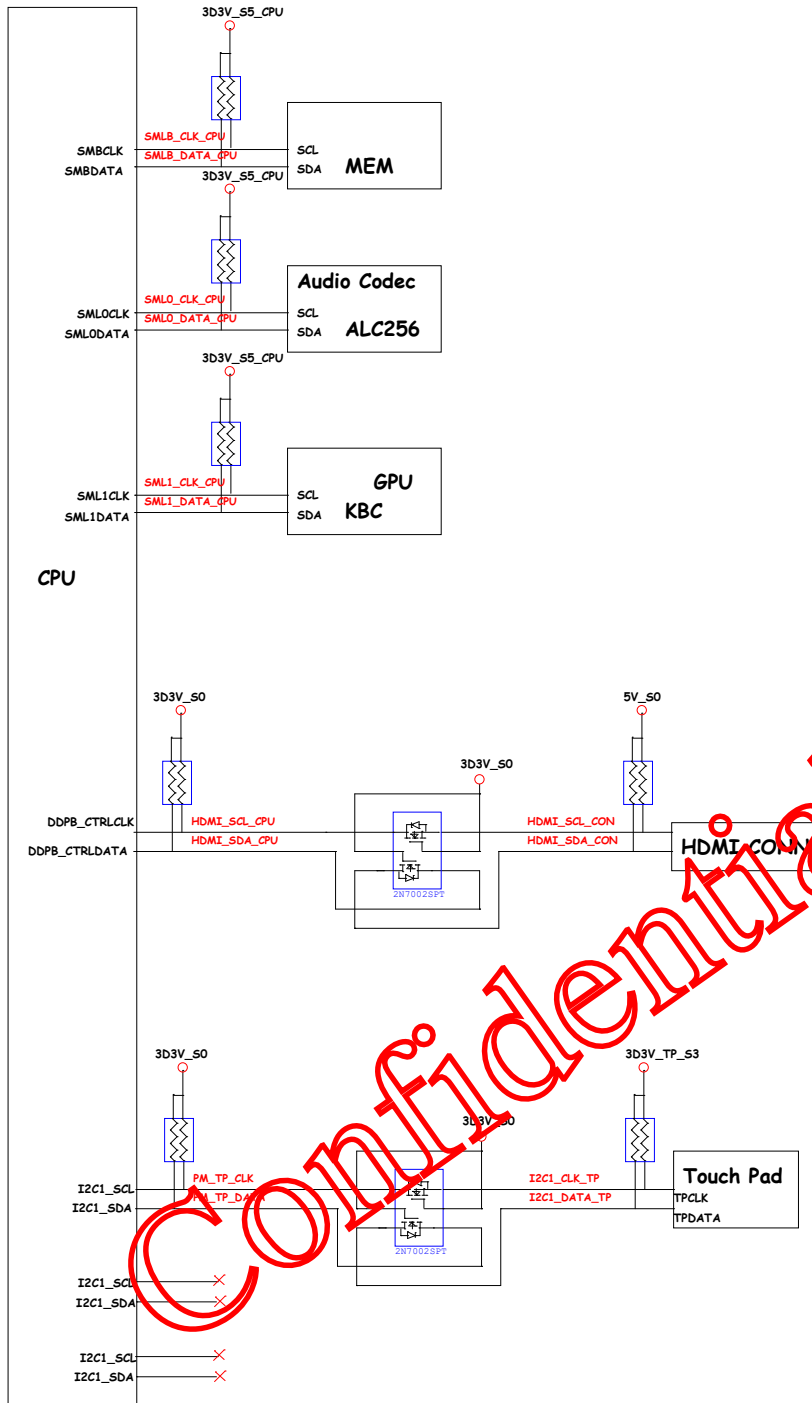


N17-Power Up Sequence

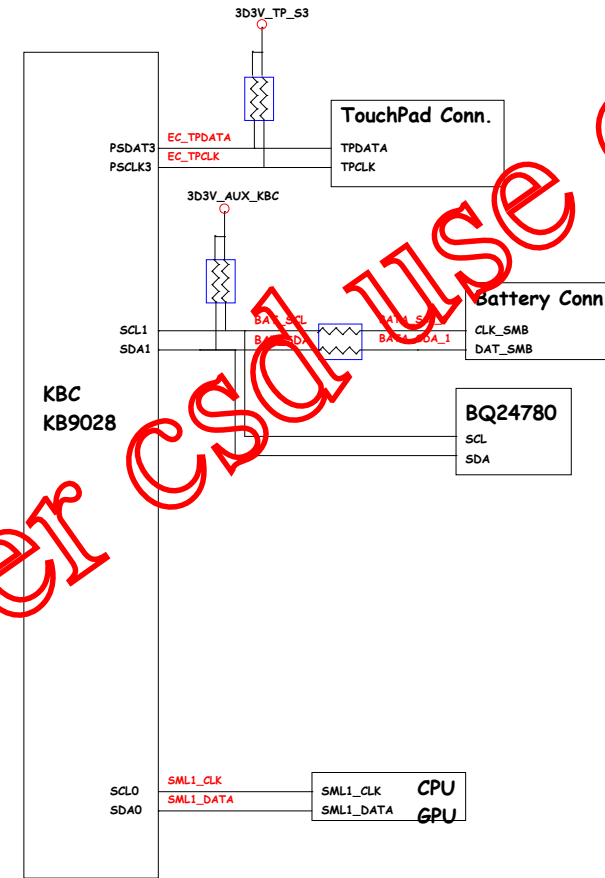




PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



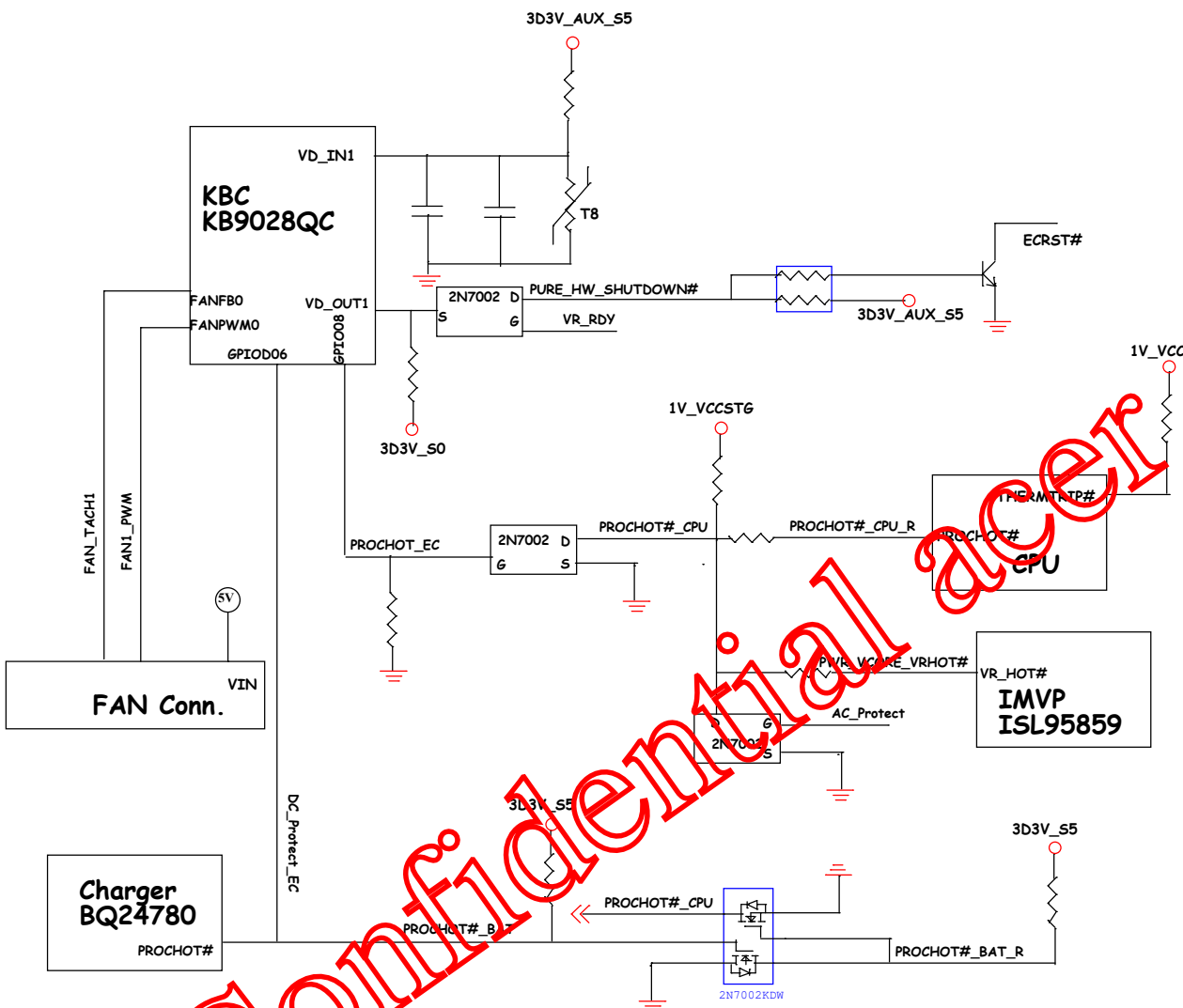
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Core Design

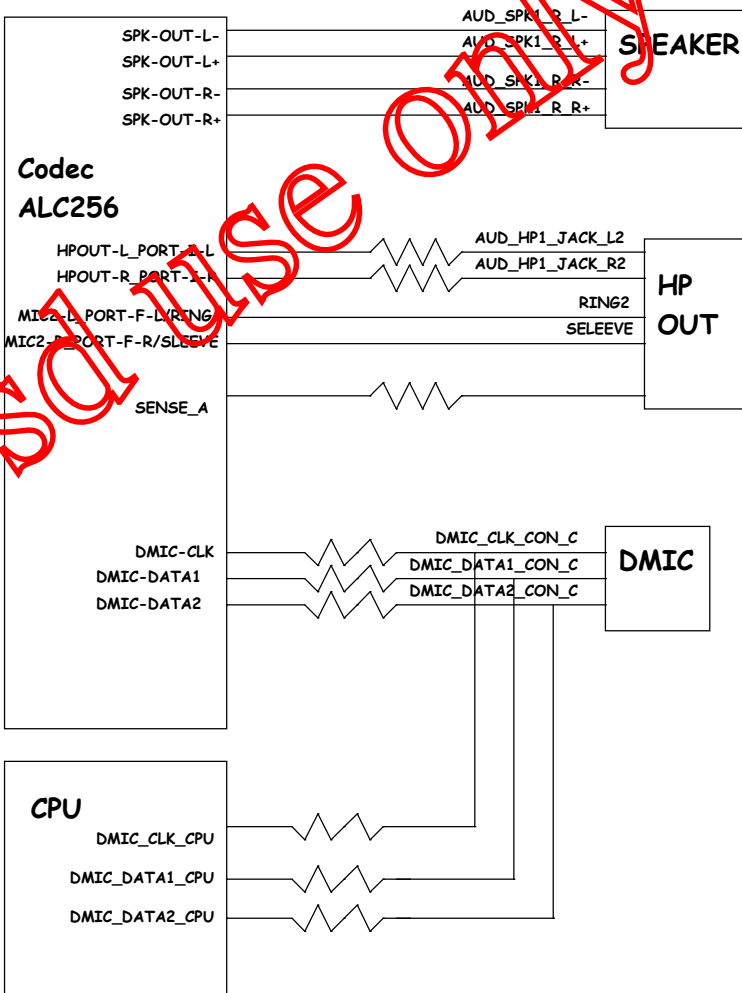
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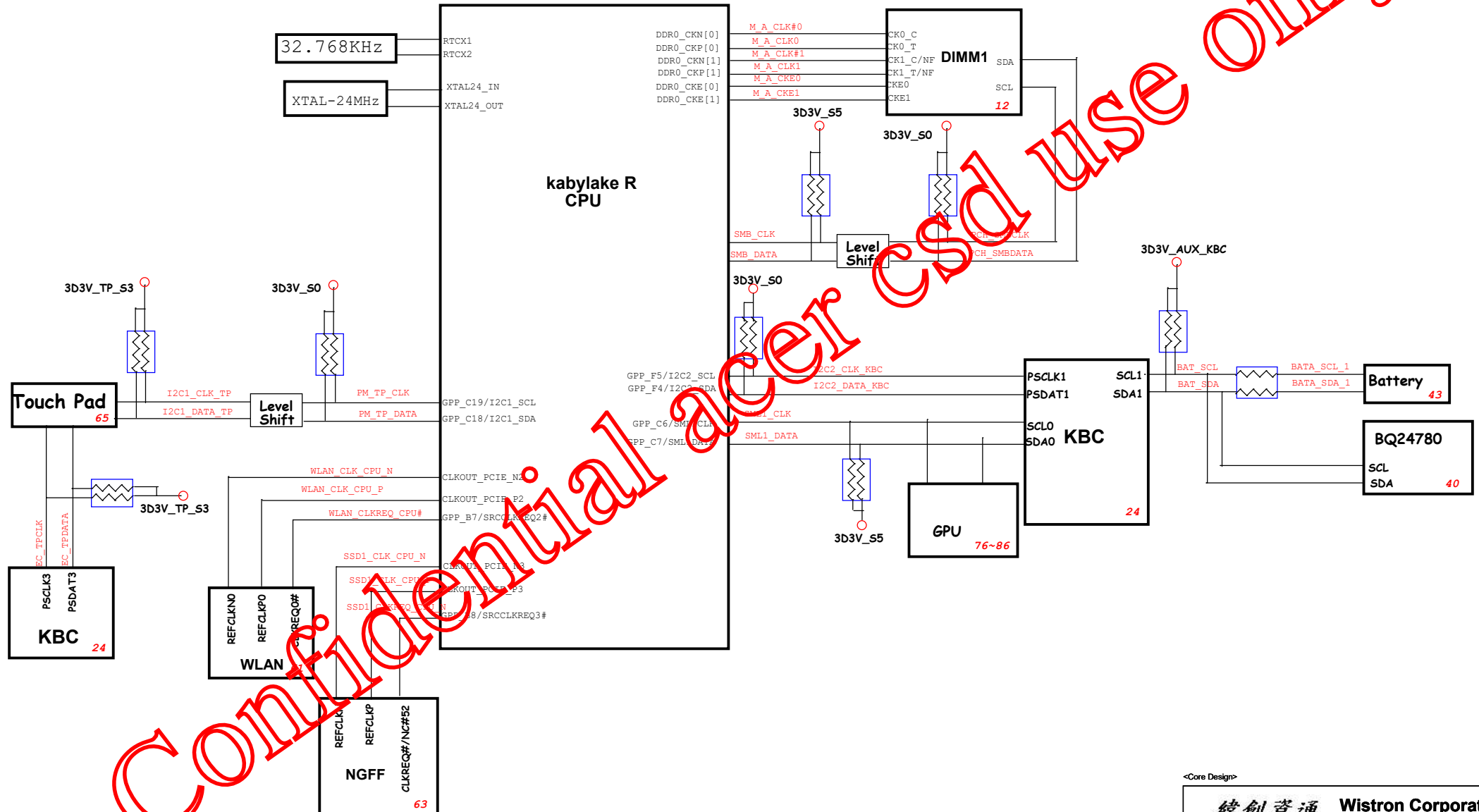
Thermal Block Diagram



Audio Block Diagram



CLOCK BLOCK DIAGRAM



<Core Design>

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